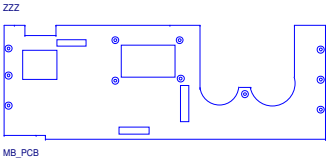


MODEL NAME : ZZZZZZ

PCB NO : LA-H931P

BOM P/N : 43xxxxx



# Dell/Compal Confidential

## Schematic Document

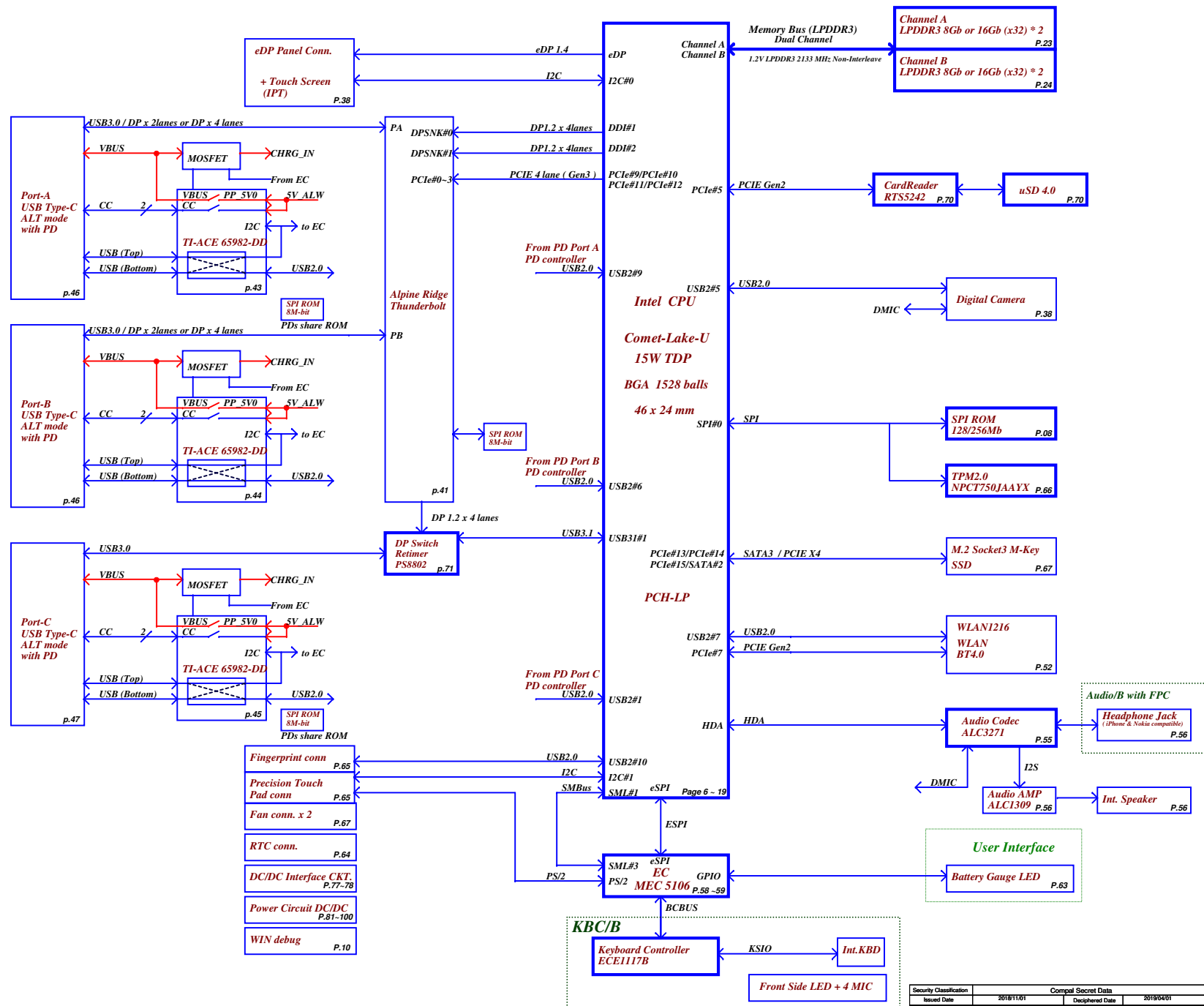
### Italia CML

2019-06-25

Rev: 0.2 ( A00)

@ : Nopop Component  
L@: Intel AX200  
XPS@ : Killer,1650w  
DCI@ : for DCI Debug  
DEBUG@ : for Other Debug  
@CONN@ : Reserve Connector Component  
@EMC@ : Reserve EMC Component  
CONN@ : Connector Component  
EMC@ : EMC Component  
RF@ : RF Solution Component  
XDP@ : XDP Debug Component  
RTD3@ : for TBT RTD3 and follow Merion  
@RTD3@ : No TBT RTD3

Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
Issued Date		Deciphered Date		Title	
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		Document Number		P01-Cover Page	
		LA-H931P		0.1	
Date: Tuesday, June 25, 2019		Sheet 1 of 100			



Board ID Table for AD channel

RE194	CE75	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	

CPU	2+2	4+2	6+2	VPro
Italia CML EDP35				

BOARD\_ID rise time is measured from 5%~68%.

SMBUS Control Table

	SOURCE	CPU VR Controller	BATTERY Charger	PD1	PD2	PD3	5106	XDP	Audio AMP	eDP	Touch Pad	Touch S	FPR
SMB00_CLK SMB00_DATA	MECS106				V								
SMB01_CLK SMB01_DATA	MECS106												V
SMB02_CLK SMB02_DATA	MECS106										V		
SMB04_CLK SMB04_DATA	MECS106			V									
SMB05_CLK SMB05_DATA	MECS106								V				
SMB06_CLK SMB06_DATA	MECS106	V											
SMB07_CLK SMB07_DATA	MECS106					V							
SMB10_CLK SMB10_DATA	MECS106		V										
PCH_SML1CLK PCH_SML1DATA	PCH						V						
SMBCLK SMBDATA	PCH							V					
I2C0_CLK I2C0_DATA	PCH											V	
I2C1_CLK I2C1_DATA	PCH										V		
I2C2_CLK I2C2_DATA	PCH									V			


PCH USB 2.0 Port Mapping	USB PORT#	DESTINATION
	1	PD PORT3
	2	NC
	3	NC
	4	NC
	5	Camera
	6	USB PD PORT2
	7	NGFF WLAN BT
	8	DCI
	9	USB PD PORT1
	10	Fingerprint
PCH USB 3.0 Port Mapping	1	DP MX (PS8802)
	2	
	3	
	4	DCI debug


PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
	2	Alpine Ridge

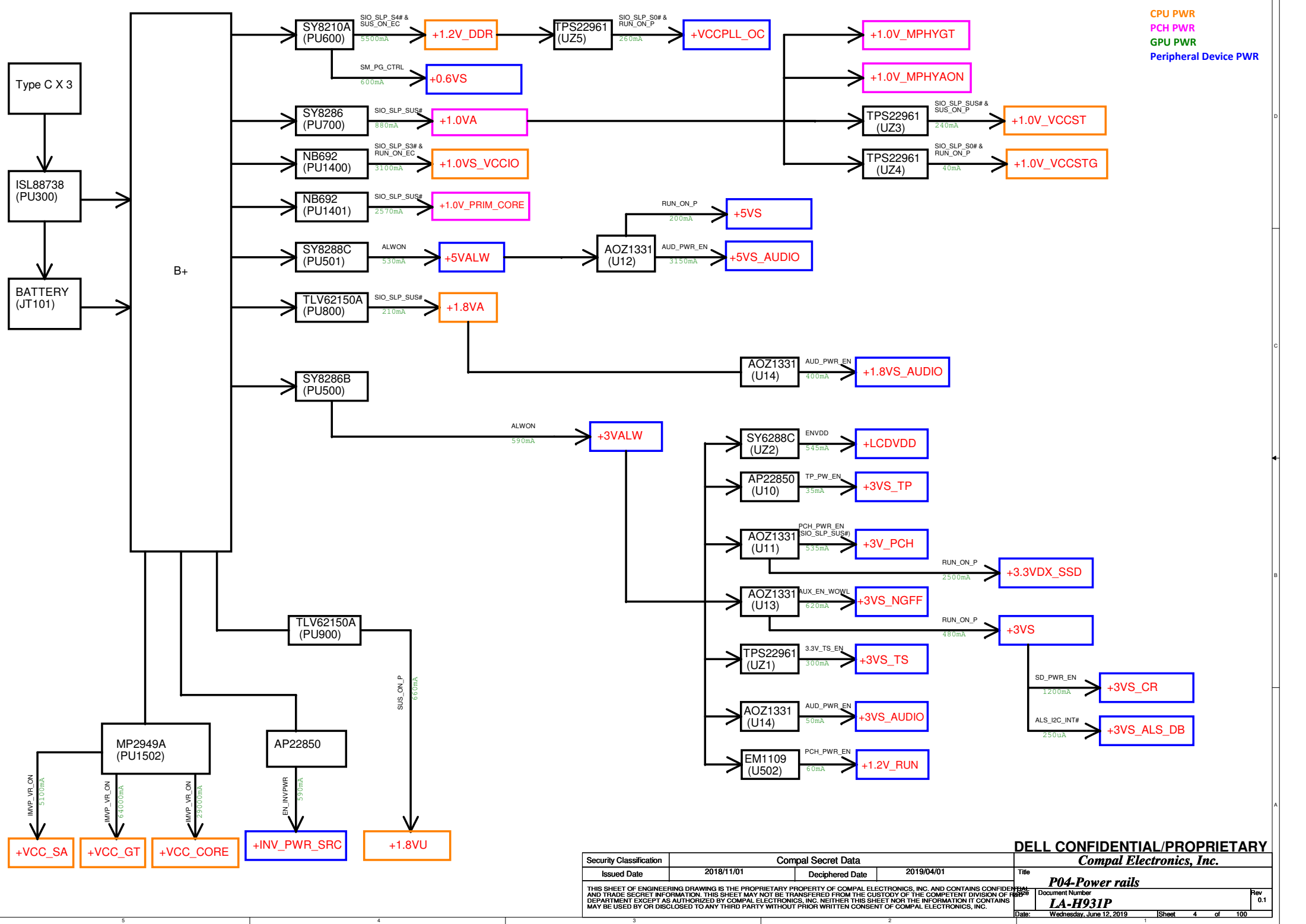
CLK	DIFFERENTIAL CLK#	DESTINATION	PCI EXPRESS PORT#	DESTINATION
	CLKOUT_PCIE0	Alpine Ridge	Lane 5	Card Reader
	CLKOUT_PCIE1	NGFF WLAN	Lane 6	NC
	CLKOUT_PCIE2	NC	Lane 7	NGFF WLAN
	CLKOUT_PCIE3	M.2 SSD	Lane 8	NC
	CLKOUT_PCIE4	NC	Lane 9	Alpine Ridge
	CLKOUT_PCIE5	Card Reader	Lane 10	Alpine Ridge
	FLEX CLK#	DESTINATION	Lane 11	Alpine Ridge
	CLKOUT_LPC_0	ESPI 5106	Lane 12	Alpine Ridge
	CLKOUT_LPC_1	NC	Lane 13	M.2 SSD
	CLKOUT_ITPXDP	XDP CONN	Lane 14	M.2 SSD
			Lane 15	M.2 SSD
			Lane 16 / SATA 2	M.2 SSD

SATA PORT#	DESTINATION
SATA-0	NC
SATA-1A	NC
SATA-1B	NC
SATA-2	M.2 SSD

Symbol Note :

 : means Digital Ground

 : means Analog Ground



# Deep Sleep

[RTC in]

[AC in]

PD Output

PD Output

+CH0\_VIN\_20V

B+

Input to EC

EC Output

EC Output

+3VALW

EC Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

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PCH Output

PCH Output

[Battery only, AC absent]

+BATT

B+

+3V\_LDOP

Input to EC

Input to EC

DC only

AC only

POWER\_SW\_IN# (AC only)

EC Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

PCH Output

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PCH Output

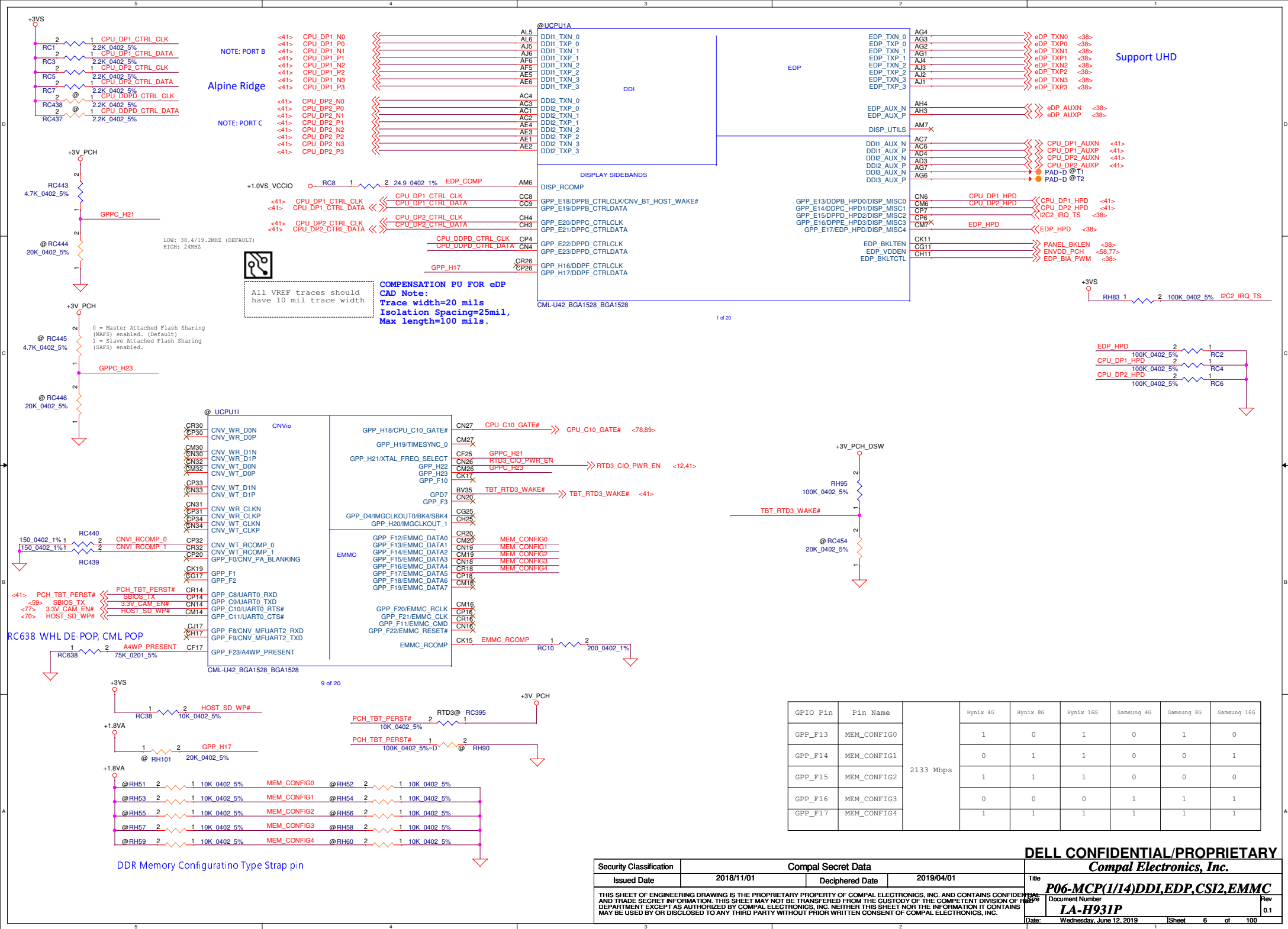
PCH Output

PCH Output

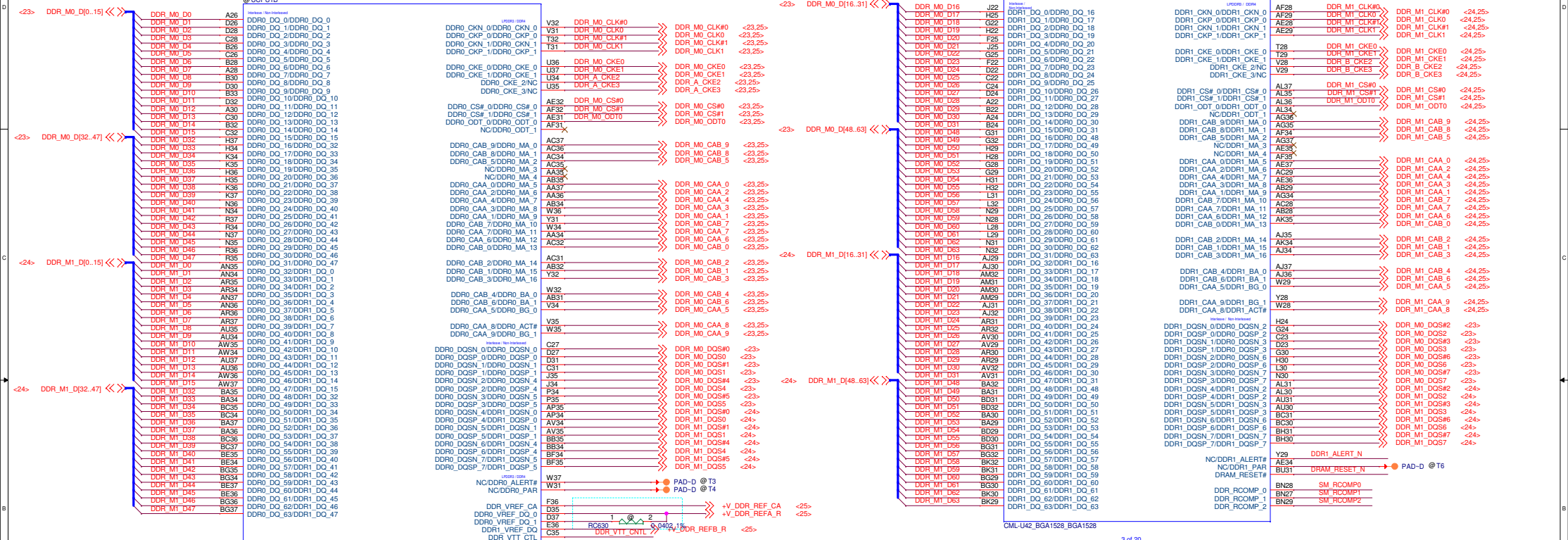
PCH Output

PCH Output

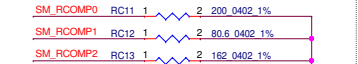
PCH Output



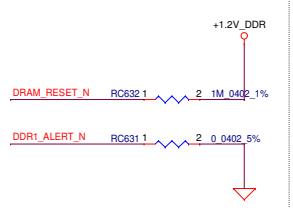
# LPDDR3, Ballout for side by side(Non-Interleave)



## LPDDR3 COMPENSATION SIGNALS



CAD Note:  
Trace width=12~15 mil, Spacing=20 mils  
Max trace length= 500 mil

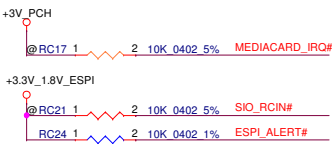
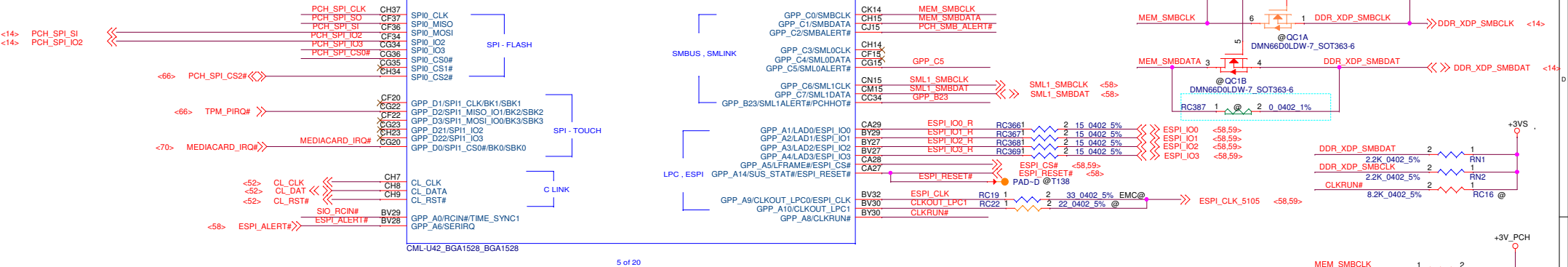


RC632 & RC631 WHL DE-POP, CML POP (FOR RVP 0.7)

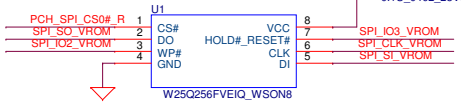
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		Date		Wednesday, June 12, 2019	
		Sheet		7 of 100	

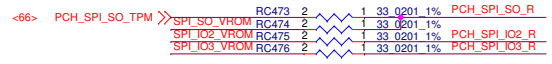
SPI\_MOSI= SPI\_IO0  
SPI\_MISO= SPI\_IO1  
PCH EDS R0.7 p.235~236



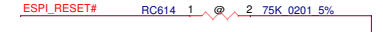
ROM is Quad SPI



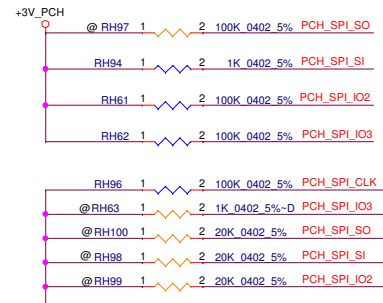
SPI ROM FOR ME ( 32 MByte )



PCH GLITCH ISSUE MITIGATION(PDG p.150)

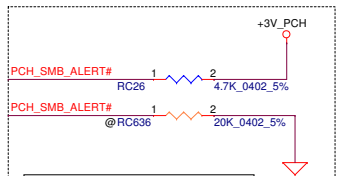
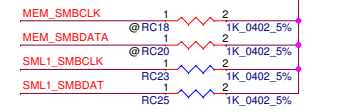


Reserve for RF

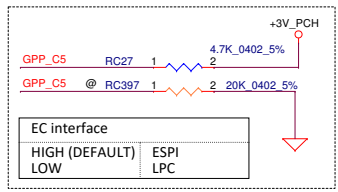


follow EDS strap chapter to pu 100 K ohm

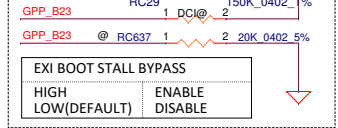
566439\_NCL\_PCH\_UY\_EDS\_Vol.1\_Rev.1.1.pdf  
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.



TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

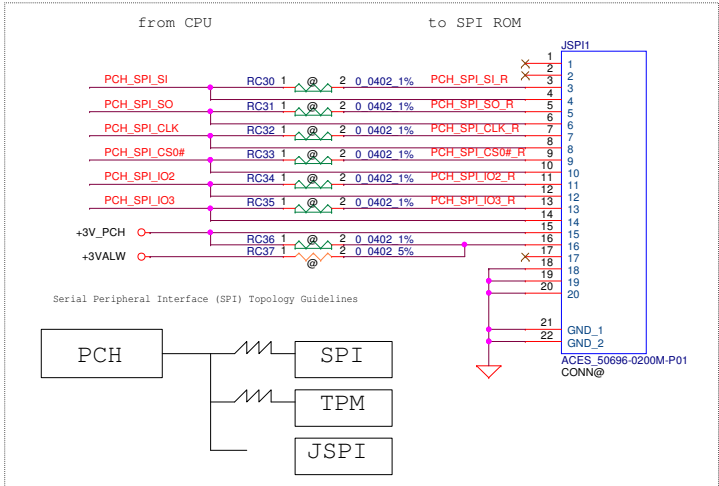


EC interface	
HIGH (DEFAULT)	ESPI
LOW	LPC



EXI BOOT STALL BYPASS	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

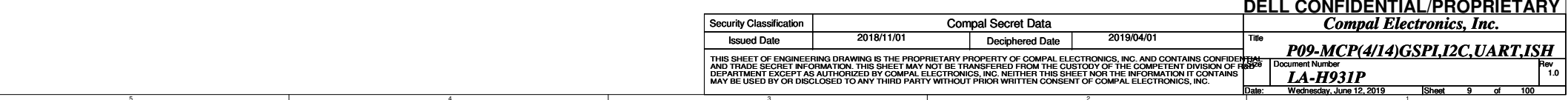
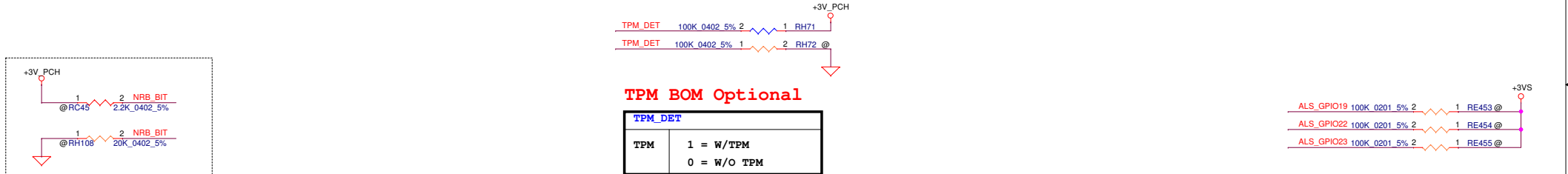
RC29 DCI need pop >100k ohm

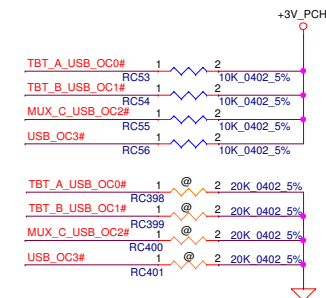
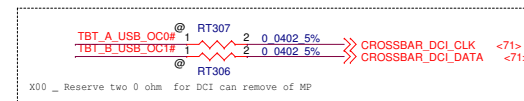
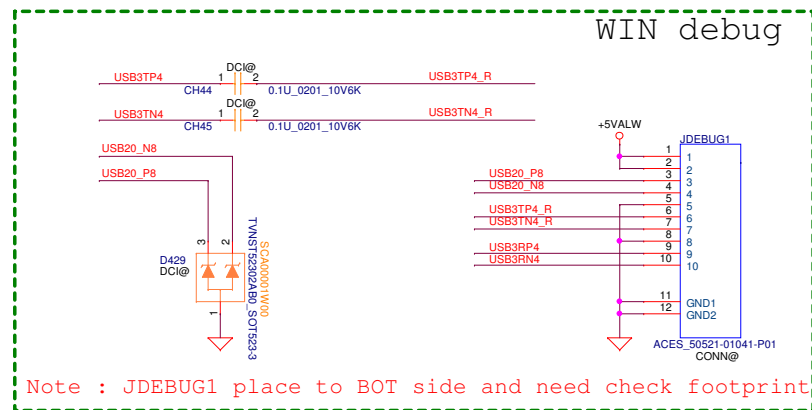
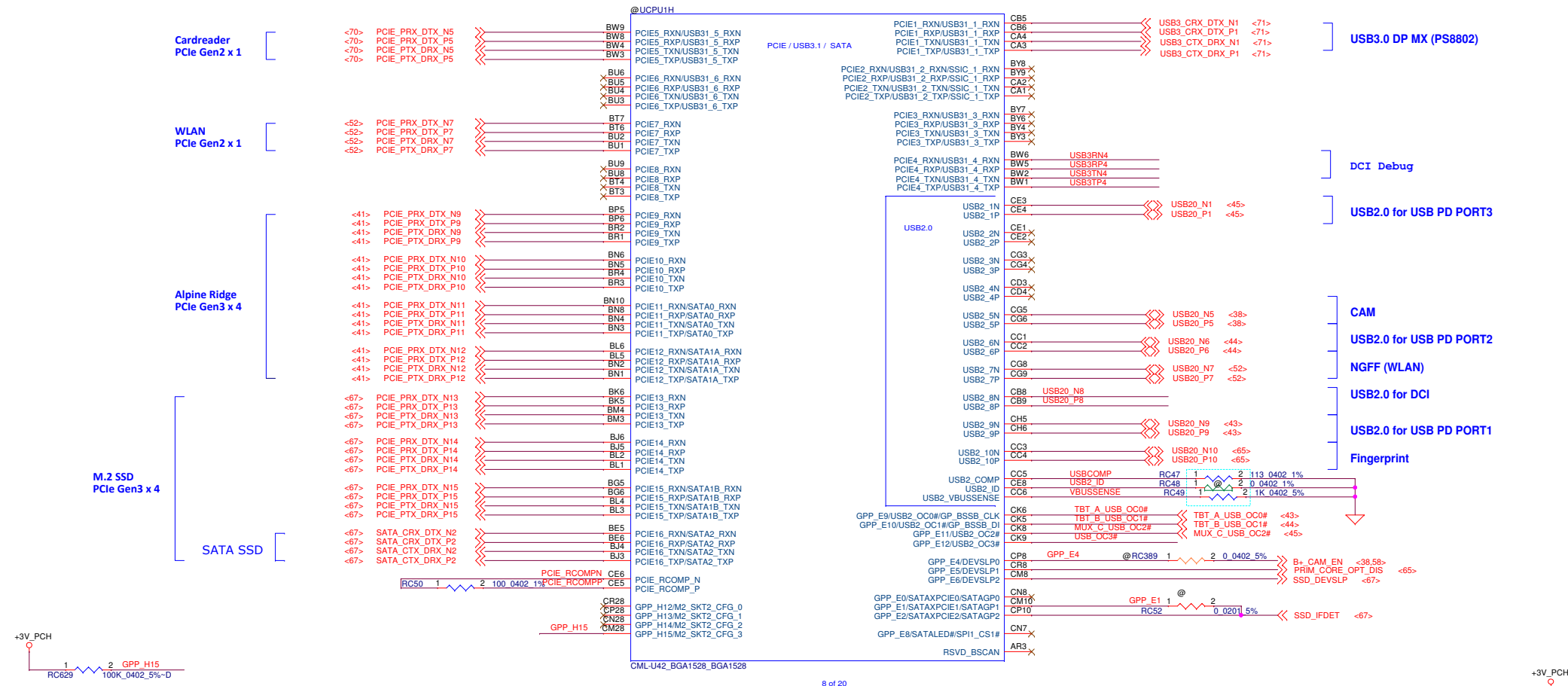


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			<b>P08-MCP(3/14)SPI,SMB,LPC</b>
			<b>LA-H931P</b>
			Rev 1.0
			Date: Wednesday, June 12, 2019
			Sheet 8 of 100

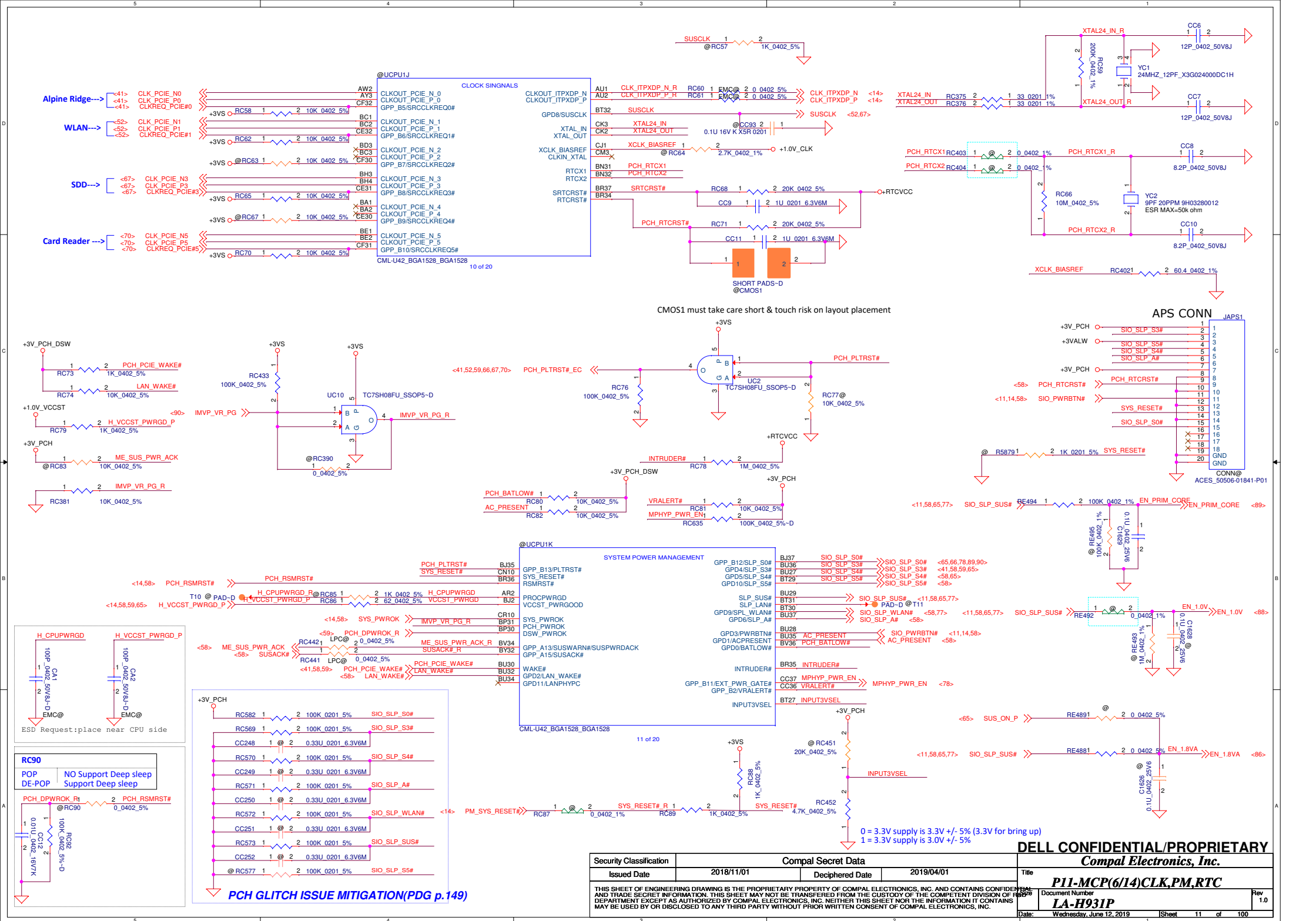
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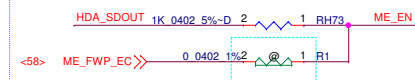
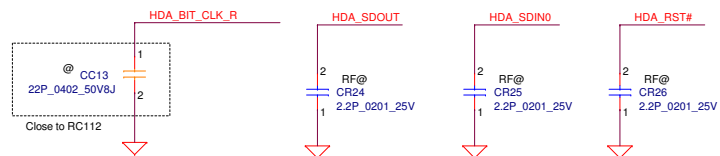




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				Document Number	LA-H931P
				Date	Wednesday, June 12, 2019
				Sheet	10 of 100

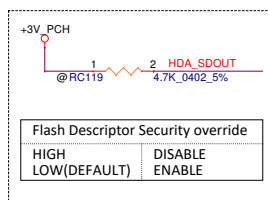
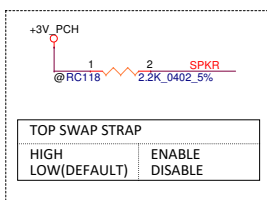
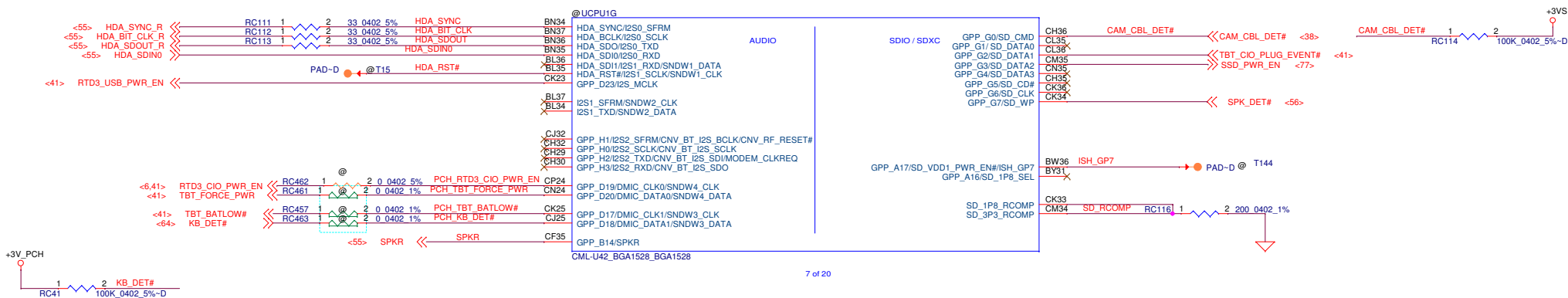


RC613 1 @ 2 100K 0201 5% HDA\_BIT\_CLK  
RC615 1 @ 2 100K 0201 5% HDA\_RST#

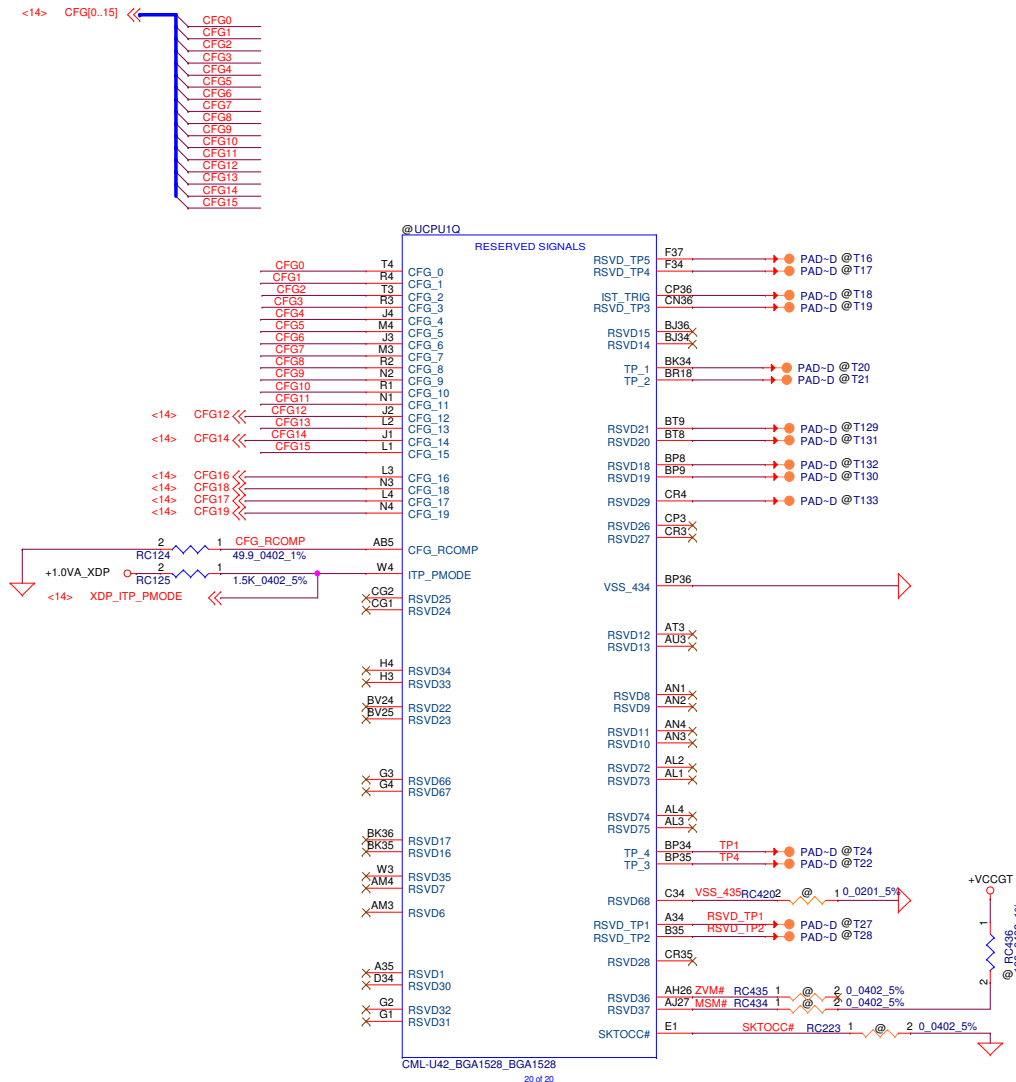
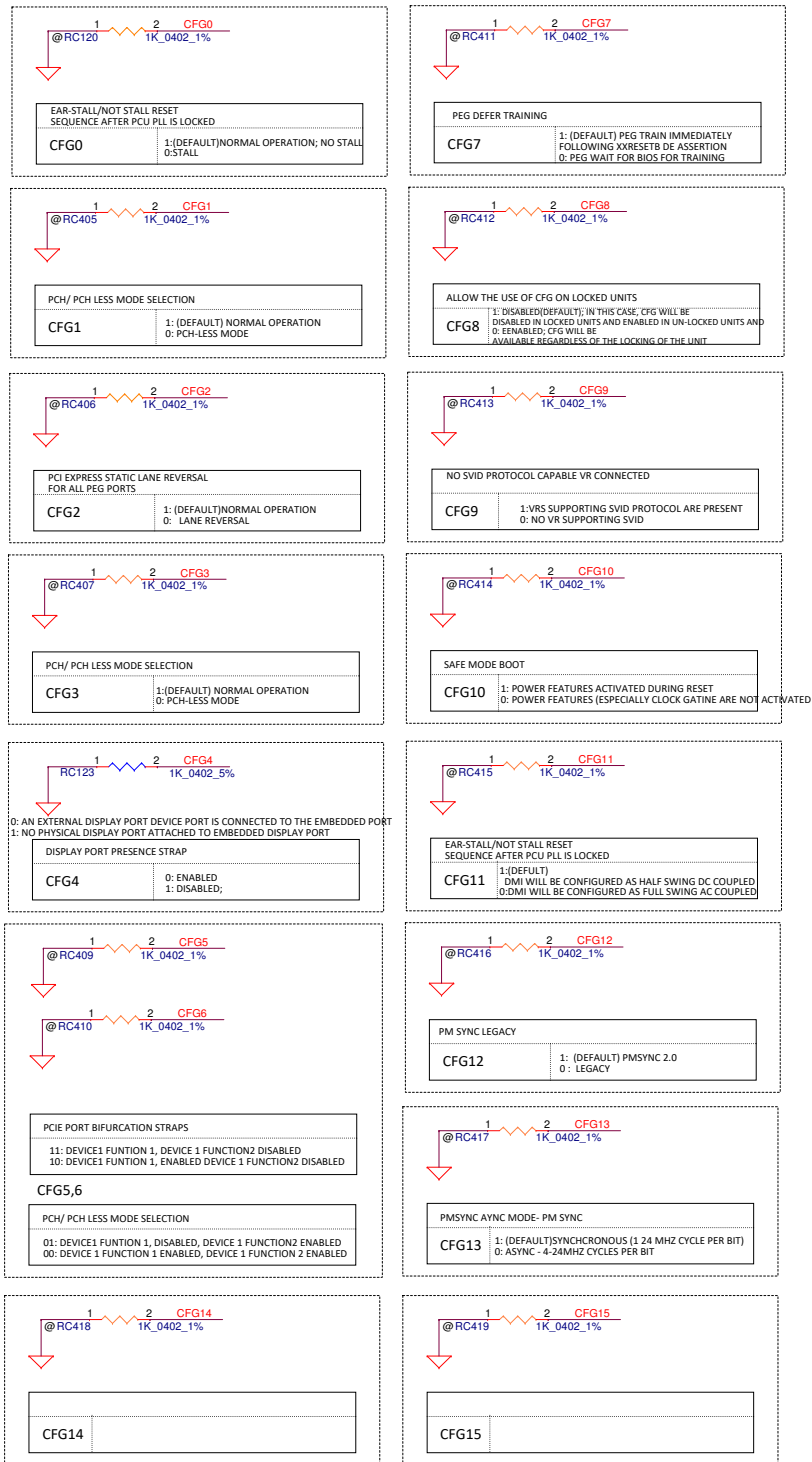


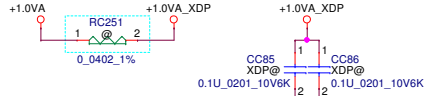
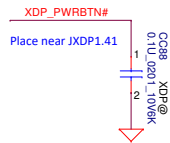
FLASH DESCRIPTOR SECURITY OVERRIDE

Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short  
Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default position)



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				Document Number		Rev	
				LA-H931P		1.0	
				Date: Wednesday, June 12, 2019		Sheet 14 of 100	

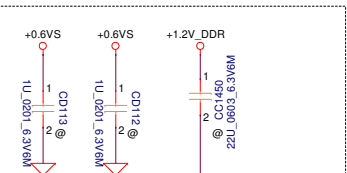
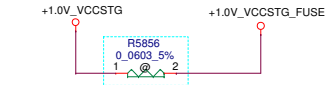
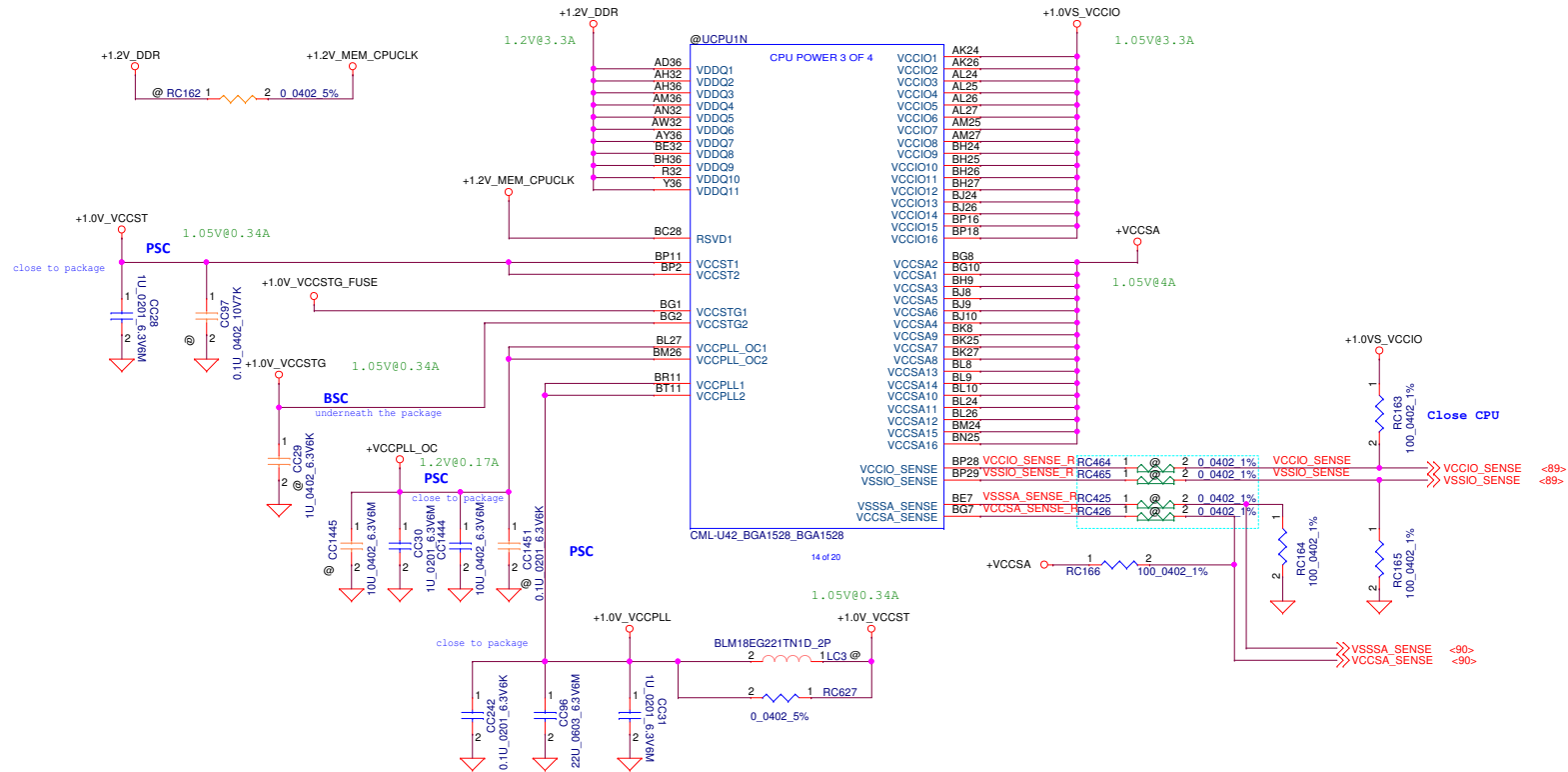




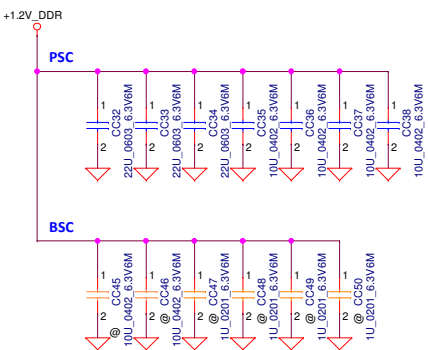




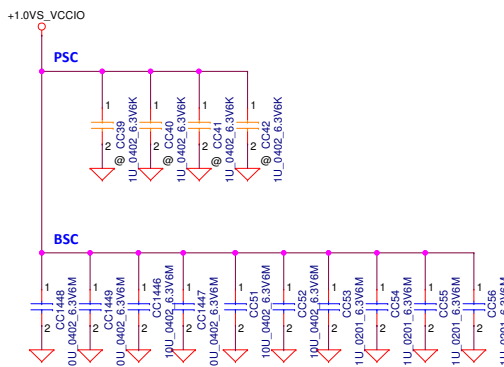
+1.2V\_DDR: 1.2V, 3.3A  
 +1.0V\_VCCST: 1.05V, 340mA  
 +1.0V\_VCCSTG: 1.05V, 120mA  
 +VCCPLL\_OC: 1.2V, 170mA  
 +1.0VS\_VCCIO: 1.05V, 3.3A  
 +VCC\_SA: 1.05V, 4A



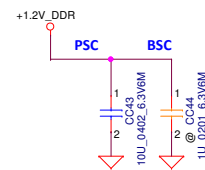
Based on Layout review with Dell  
 EE for DDR issue ,  
 add a PSC capacitor with +1.2V\_DDR  
 for reserve .  
 Not follow RVP 07/26 / can  
 remove it.



**+1.2V\_DDR Decoupling Requirement**  
 Back Side (underneath the package):  
 10U\_0402\*2 pcs + 1U\_0201\*4 pcs (8)  
 Primary Side (close to package):  
 10U\_0402\*4 pcs + 22U\_0603\*3 pcs



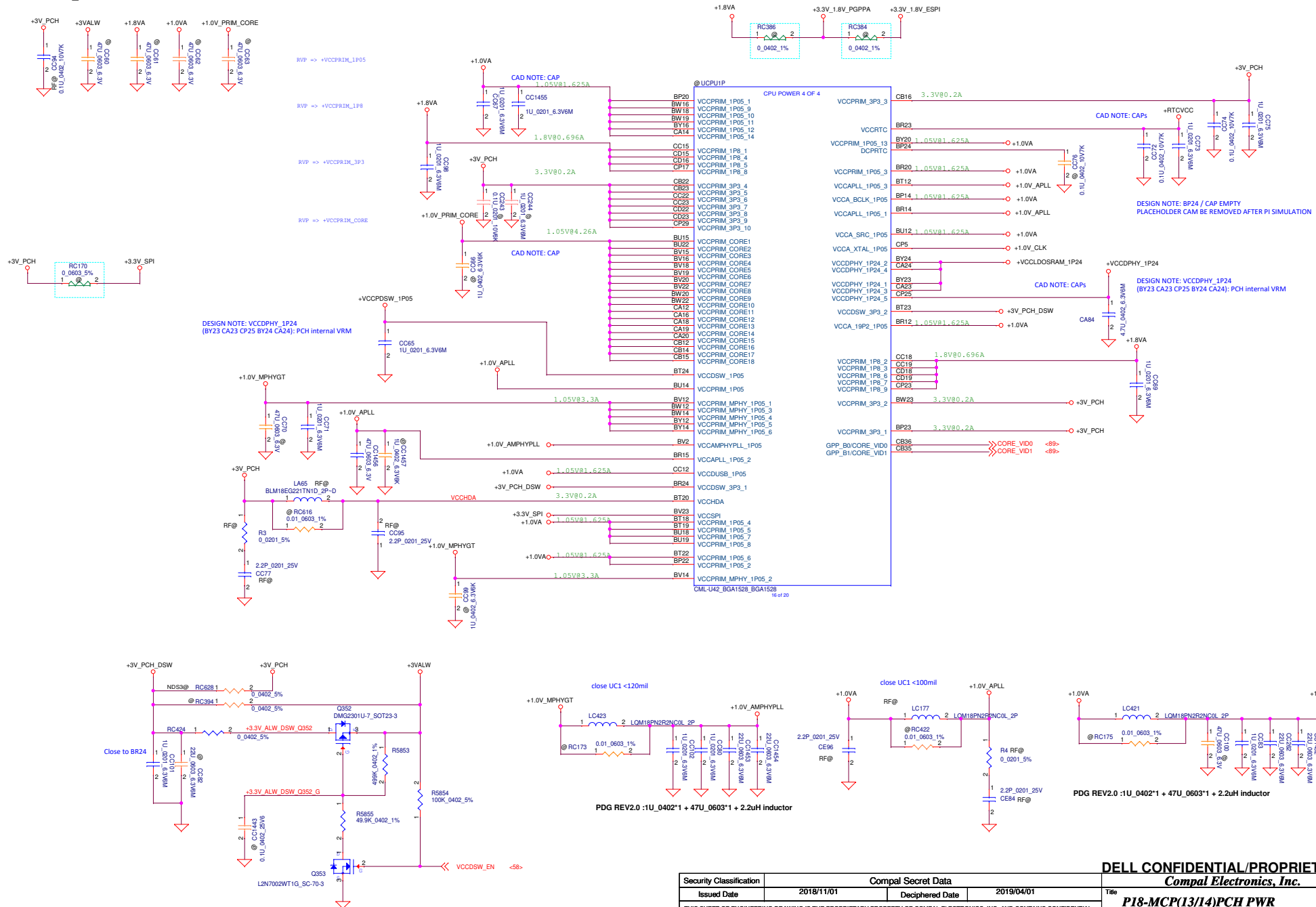
**+1.0VS\_VCCIO Decoupling Requirement Back Side**  
 (underneath the package):  
 10U\_0402 \* 6 pcs +  
 1U\_0201 \* 4 pcs  
 Primary Side (close to package):  
 1U\_0402 \*4 pcs (8) (Placeholder Only)



+1.2V\_MEM\_CPUCLK (VDDQC) Place on CPU  
 Back Side (underneath the package):  
 1U\_0201\*1 pcs (8)  
 Primary Side (close to package):  
 10U\_0402 \* 1 pcs

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Title	P17-MCP(12/14)PWR-VCCIO, MEM		
Document Number	LA-H931P		
Date	Monday, June 17, 2019	Sheet	17 of 100

**PCH PWR**



**Compal Electronics, Inc.**

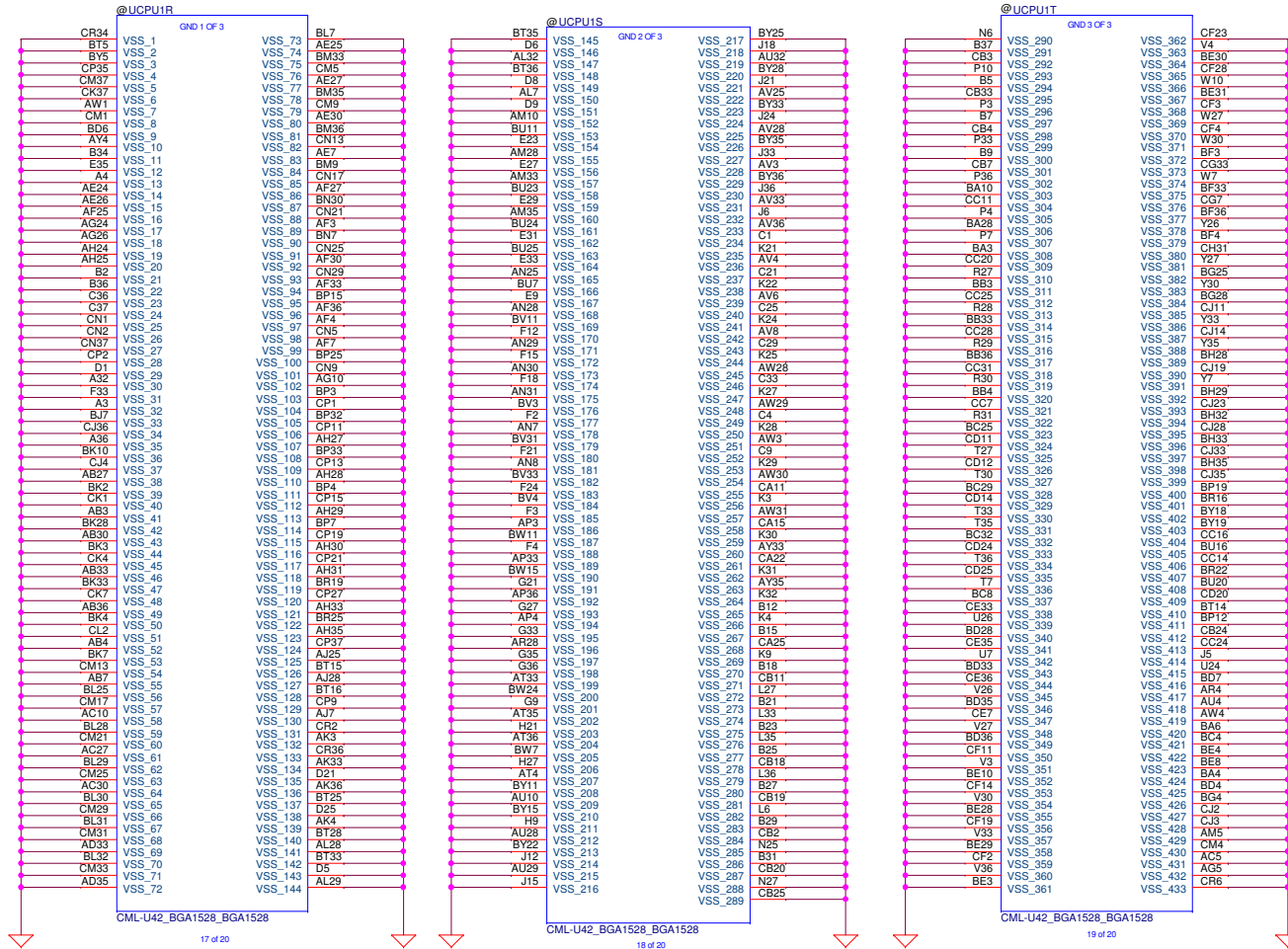
**P18-MCP(13/14)PCH PWR**

Document Number  
**LA-H931P**

Date:	Monday, June 17, 2019	Sheet	18	of	100
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Note1: VCCPRIM\_CORE Implementation with PCH CORE\_VID Recommendation





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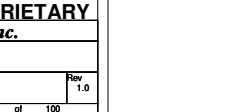
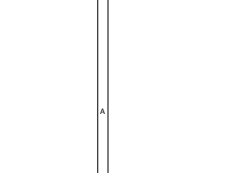
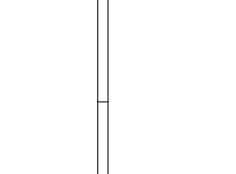
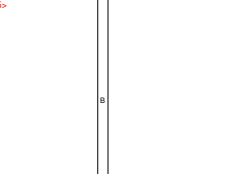
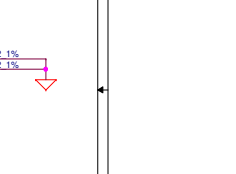
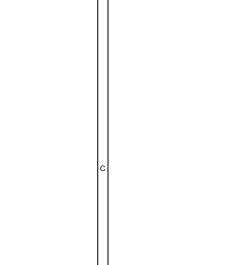
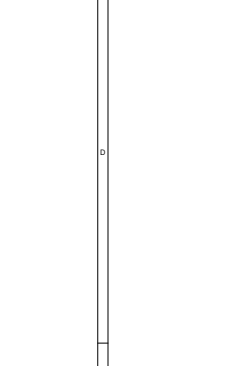
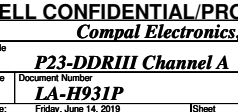
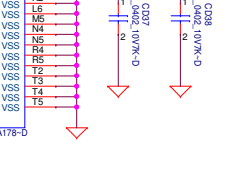
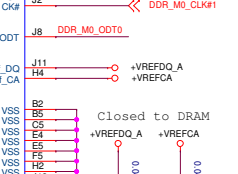
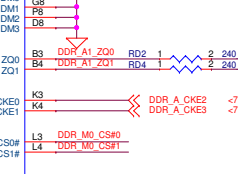
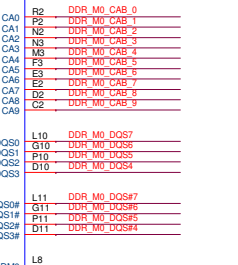
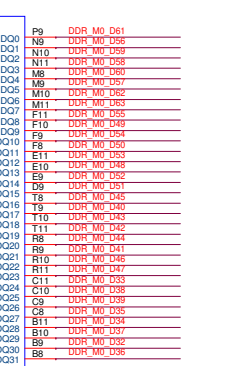
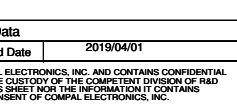
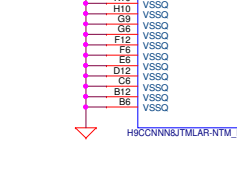
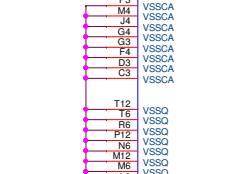
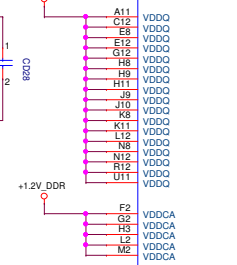
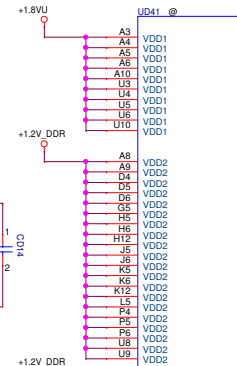
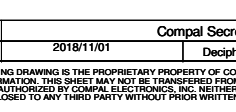
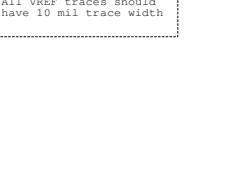
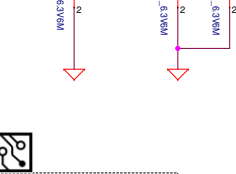
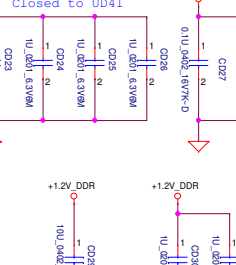
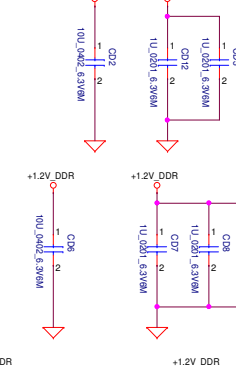
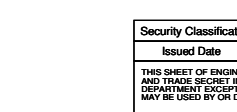
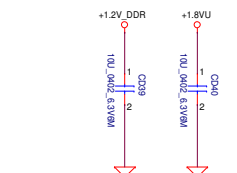
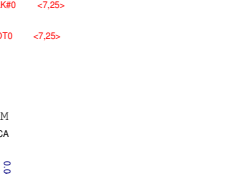
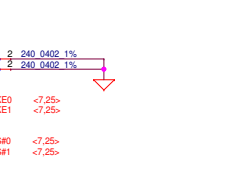
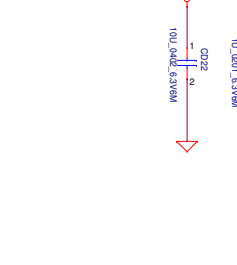
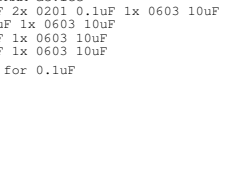
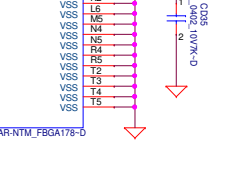
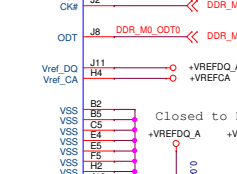
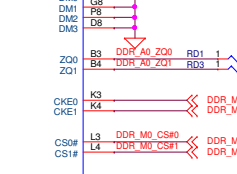
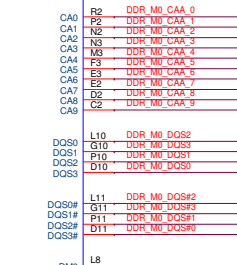
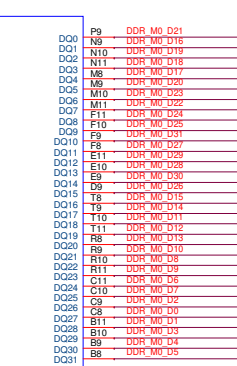
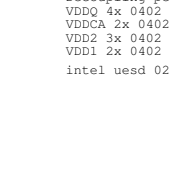
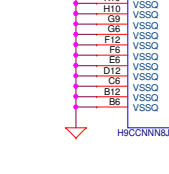
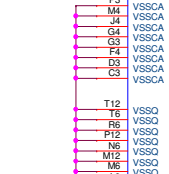
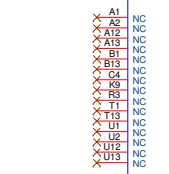
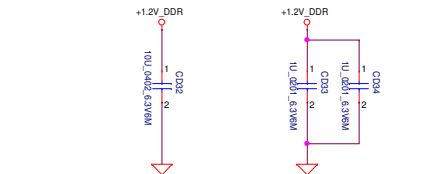
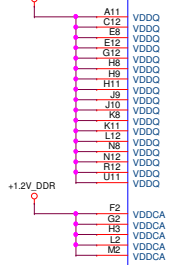
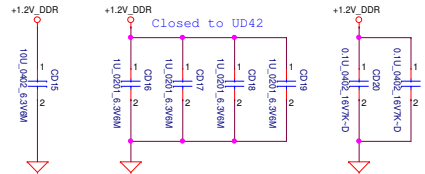
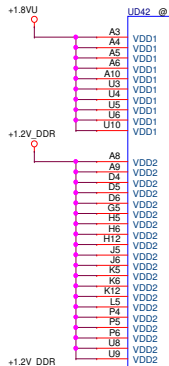
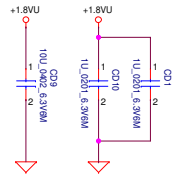


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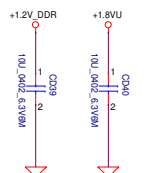


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				P022 - Reserve							
				Size	Document Number						
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+1.2V\_DDR: 1.2V, 2.04A  
+1.8VU: 1.8V, 40mA



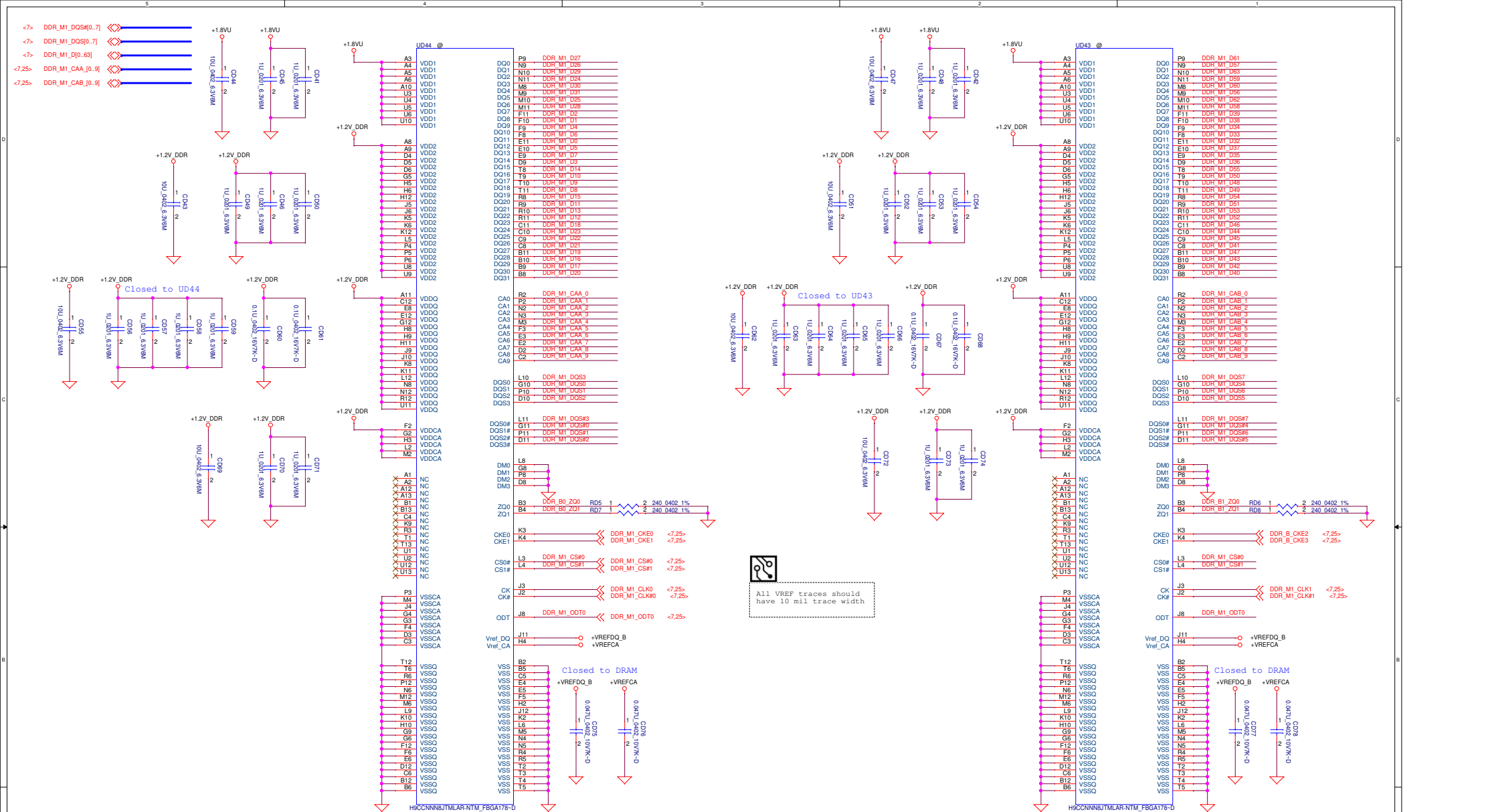
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VDD1 2x 0402 1uF 1x 0603 10uF  
intel used 0201 for 0.1uF



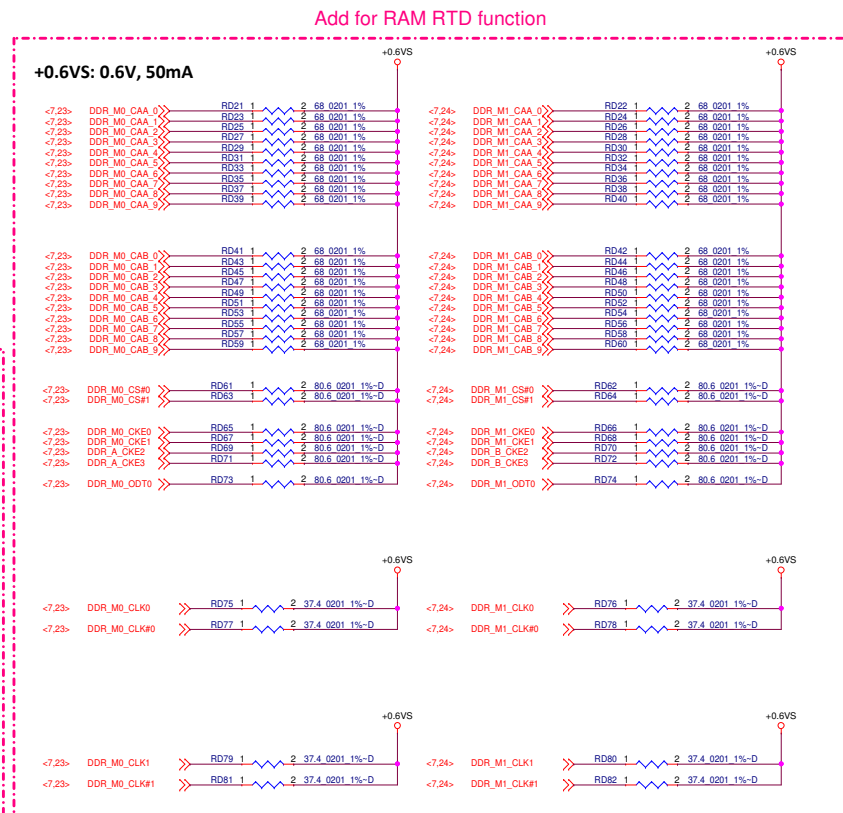
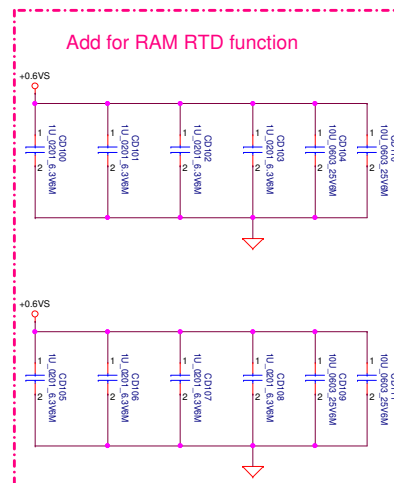
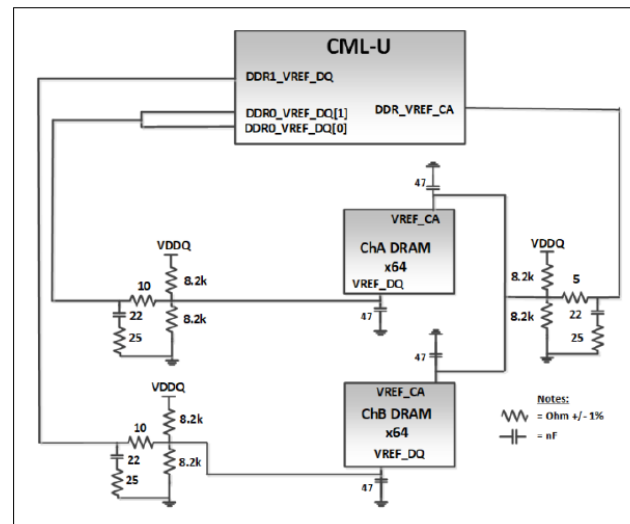
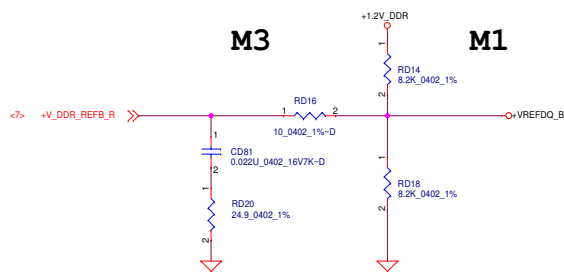
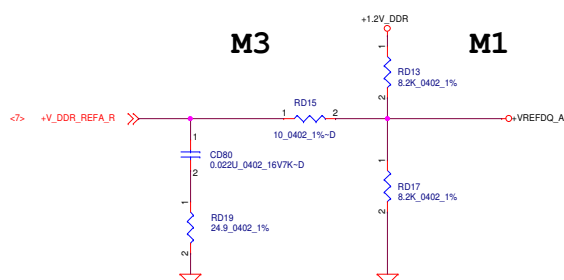
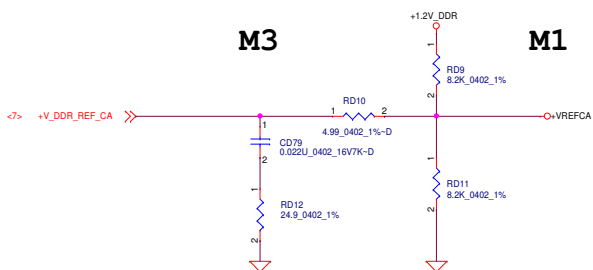
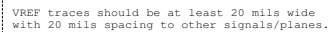
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				Size	Document Number
				LA-H931P	
				Date:	Wednesday, June 12, 2019
		Sheet	35	of	100

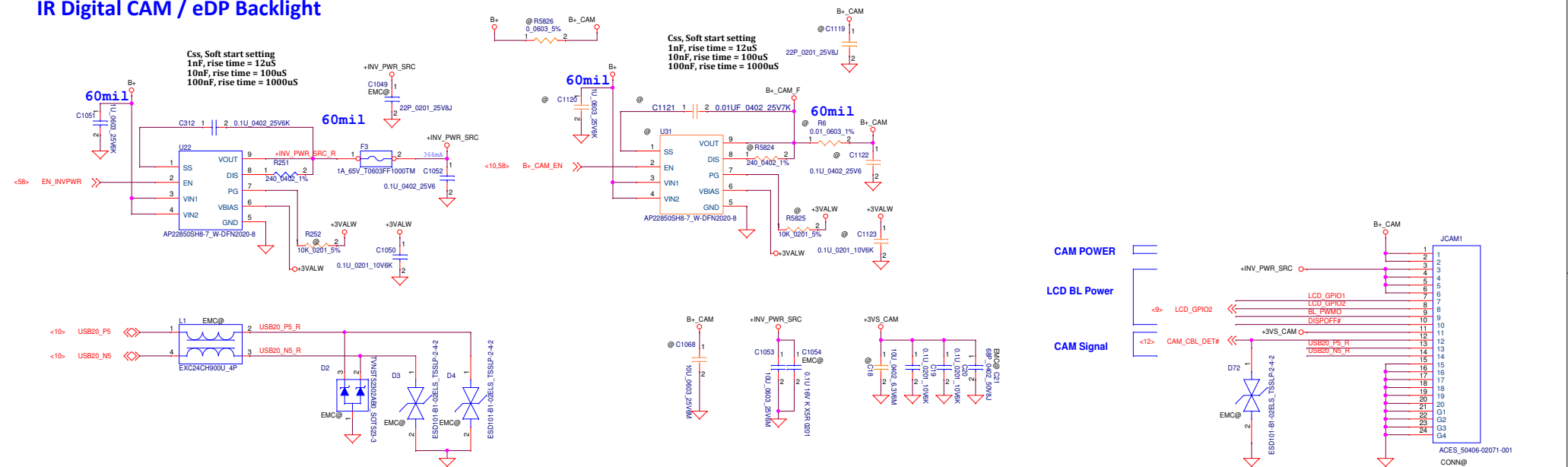


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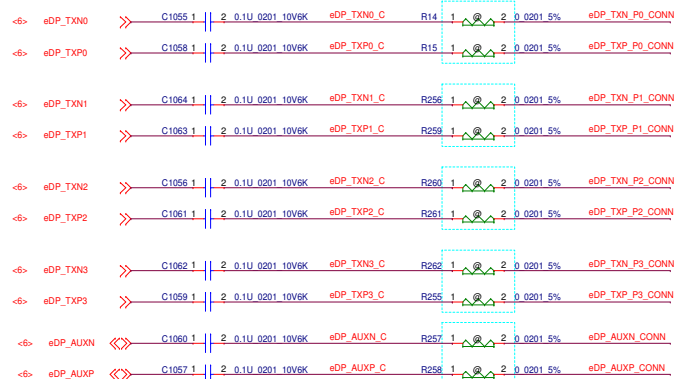


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				Sheet	37 of 100
				Rev	0.1

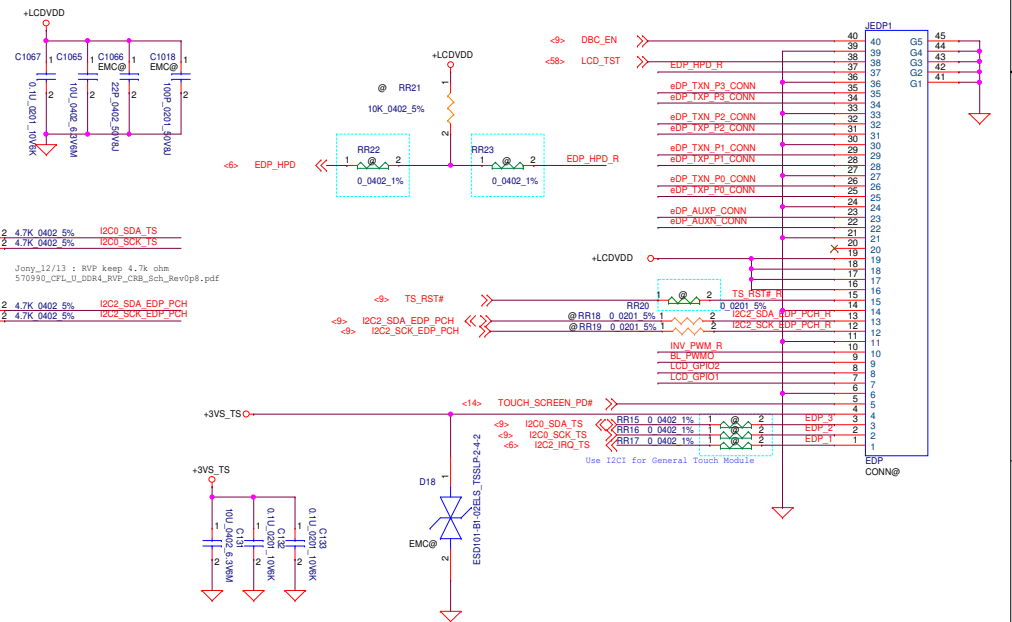
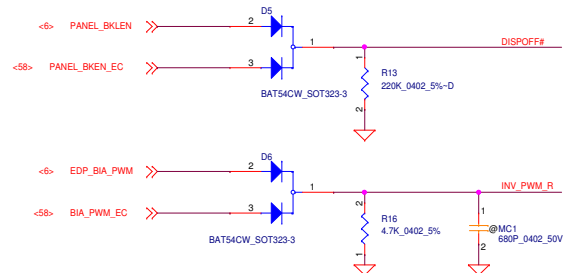
# IR Digital CAM / eDP Backlight



## eDP Conn



## BackLight PWM Control



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				LA-H931P
				Rev 1.0
				Date: Friday, June 14, 2019
				Sheet 38 of 100



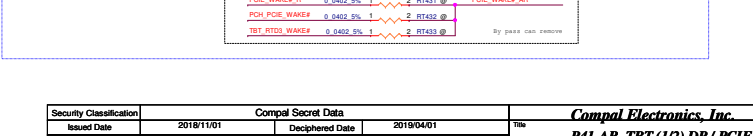
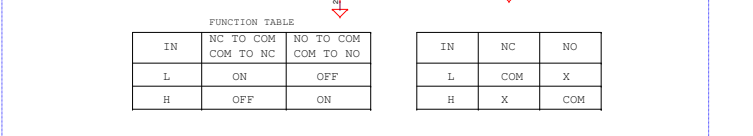
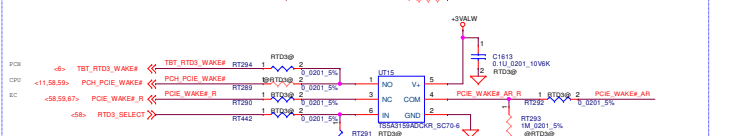
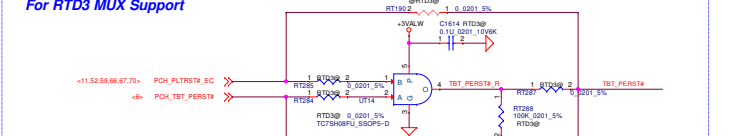
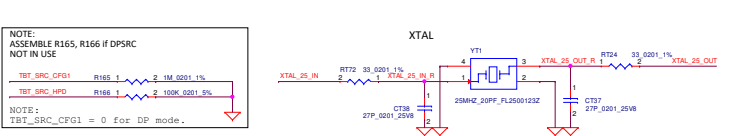
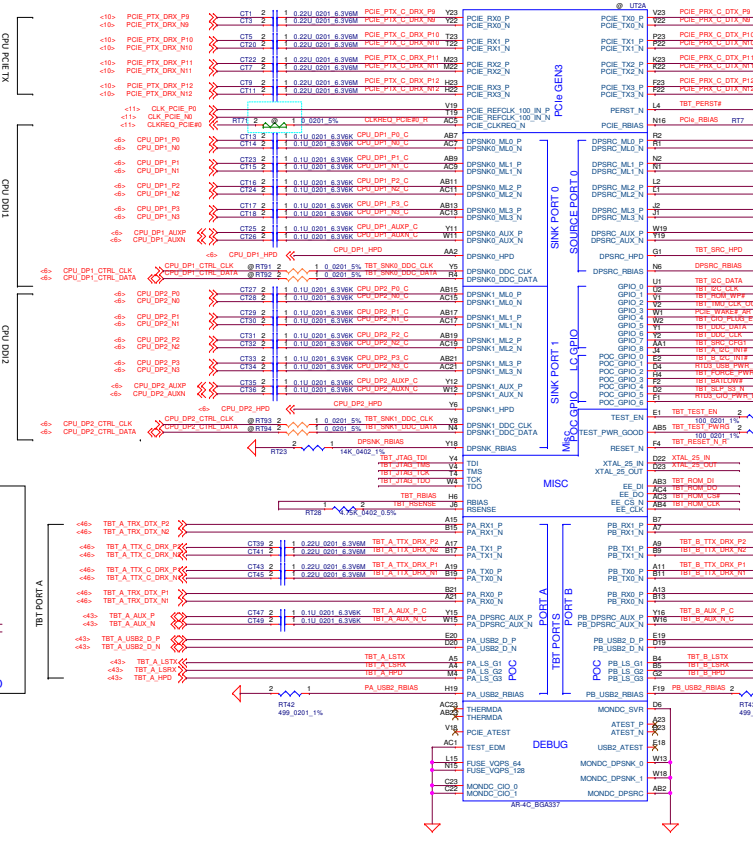
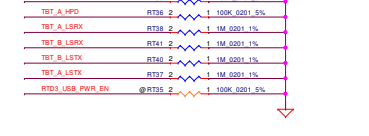
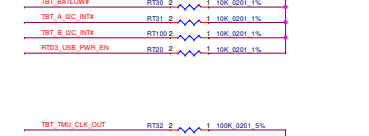
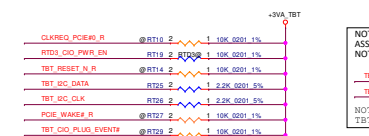
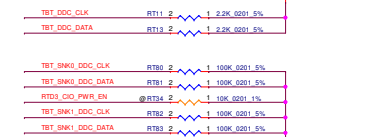
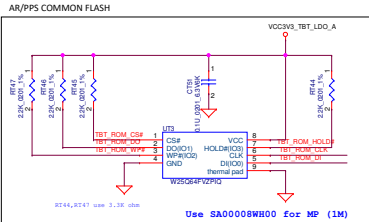
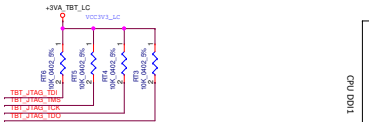
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Date: Wednesday, June 12, 2019				Sheet	39 of 100	



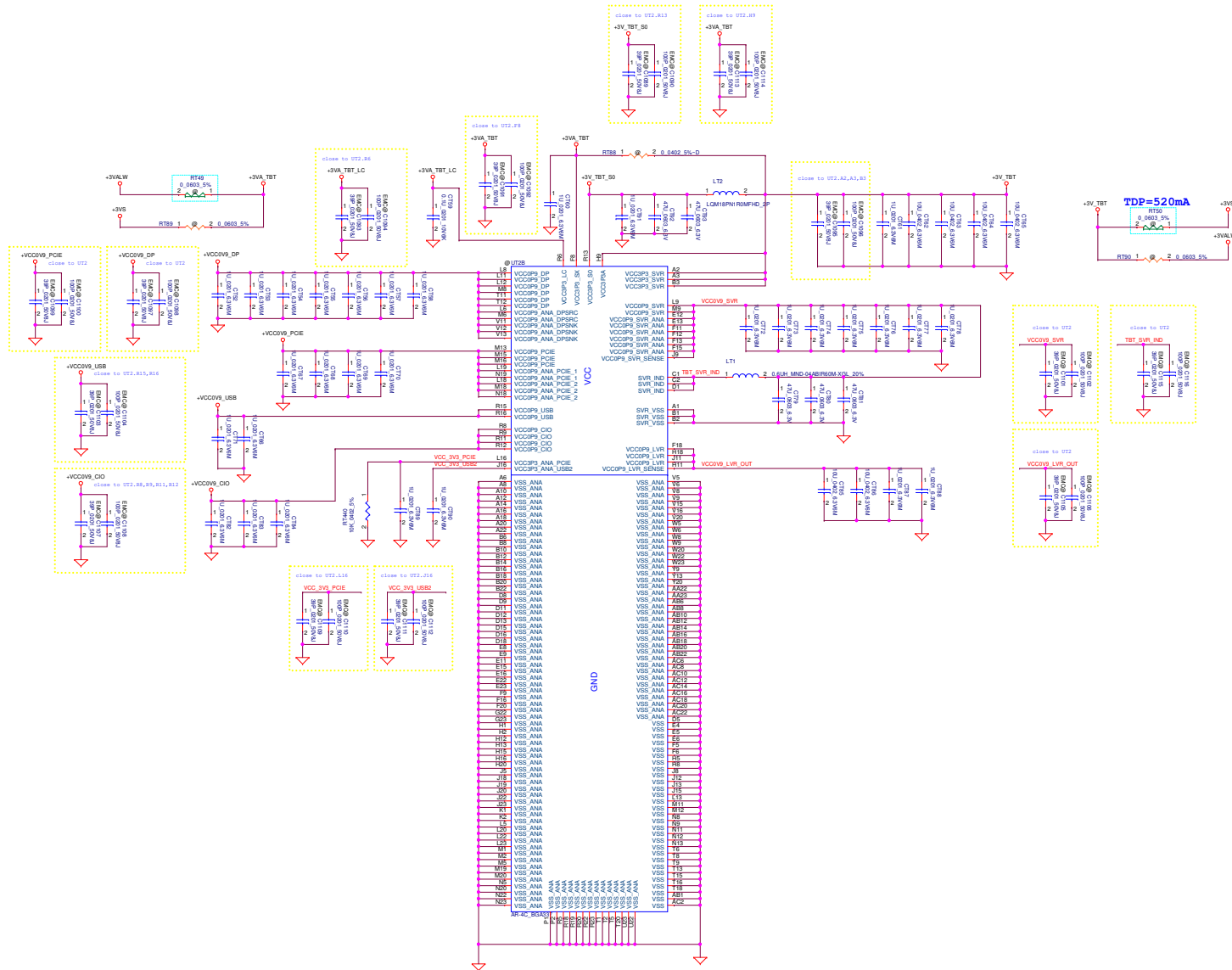
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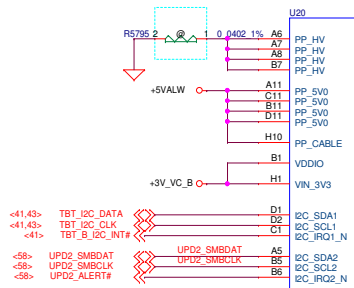
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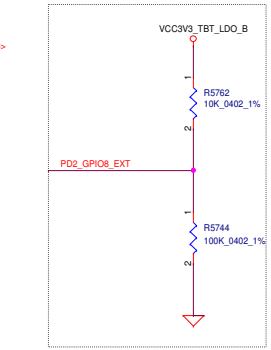






Timing diagram showing signals and their connections:

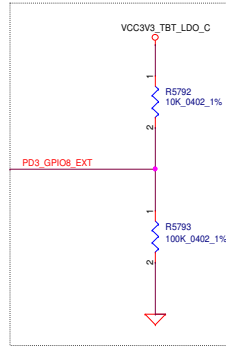
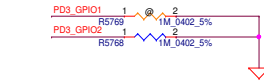
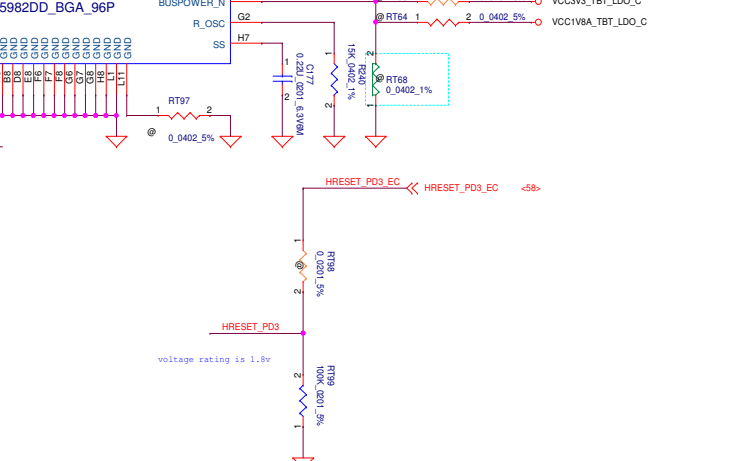
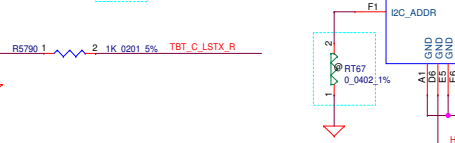
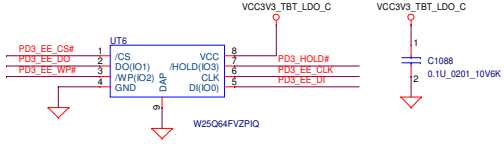
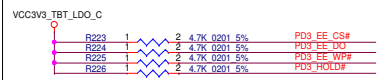
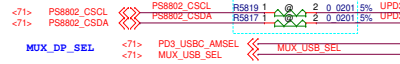
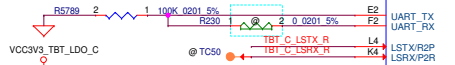
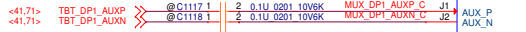
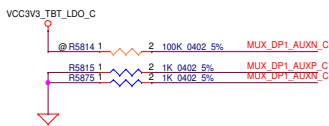
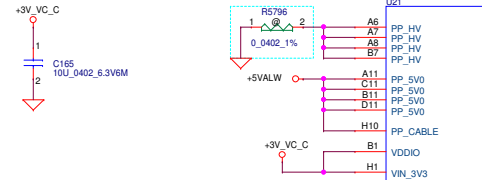
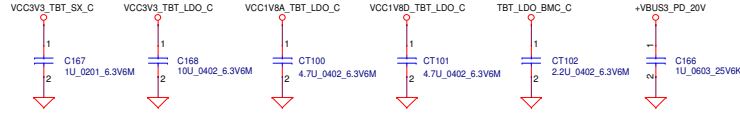
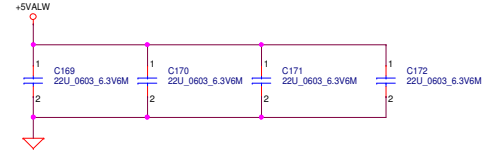
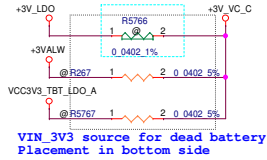
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- PD1 EE DT (R5779) → SPI\_MOSI
- PD1 EE DO (R5780) → SPI\_MISO
- PD1 EE CS# (R5781) → SPI\_SS
- PD2 EE CLK (A3) → TBT\_USR80 P6
- PD2 EE DT (B4) → TBT\_USR820 N6
- PD2 EE DO (B5) → TBT\_B\_AUX\_P
- PD2 EE CS# (B3) → TBT\_B\_AUX\_N
- TBT\_USR80 P6 → L5
- TBT\_USR820 N6 → K5
- TBT\_B\_AUX\_P → J1
- TBT\_B\_AUX\_N → J2
- L5 → USB\_RP\_P
- K5 → USB\_RP\_N
- J1 → AUX\_P
- J2 → AUX\_N

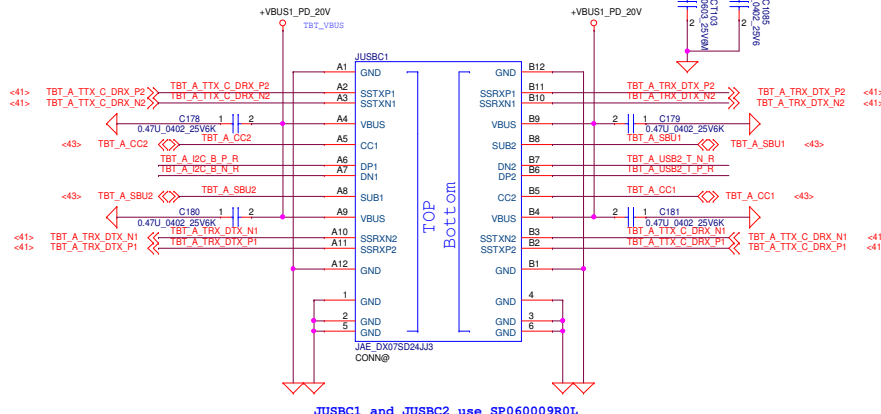
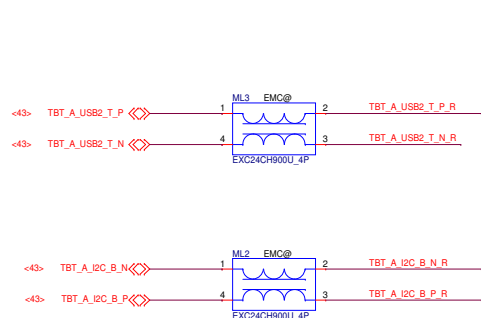


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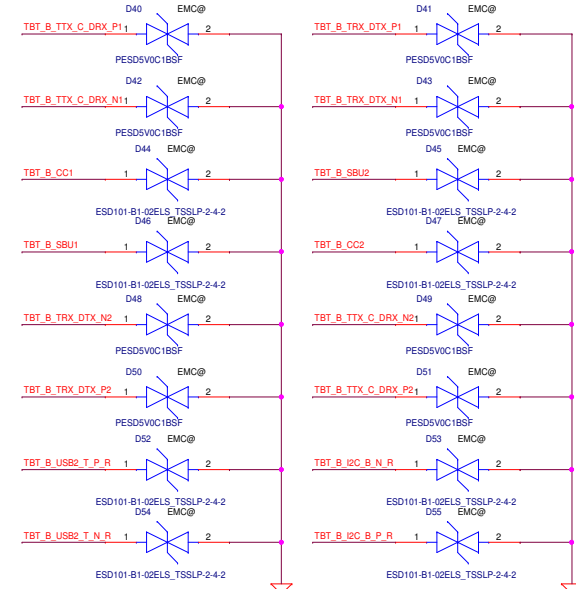
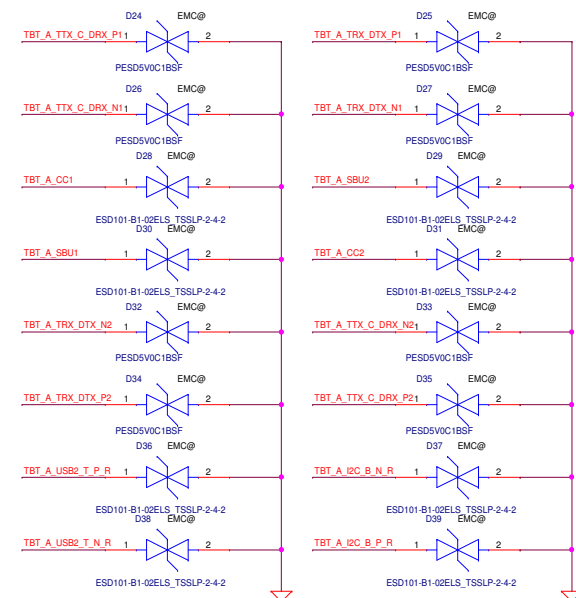
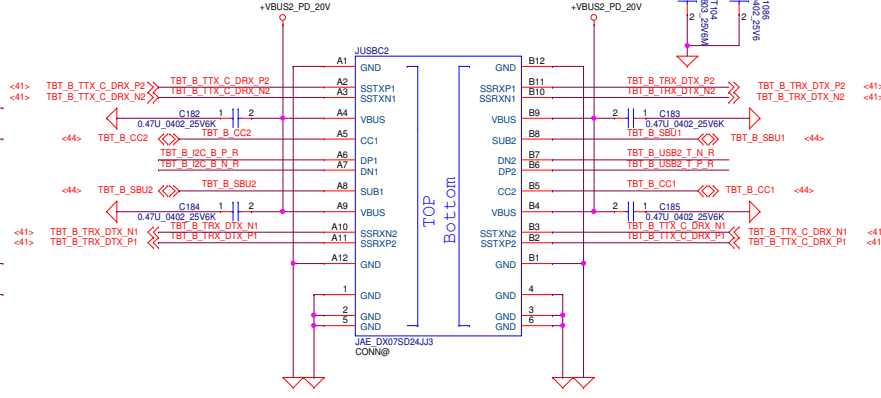
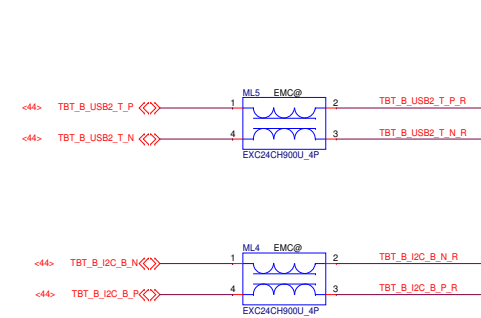
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				Product	721P
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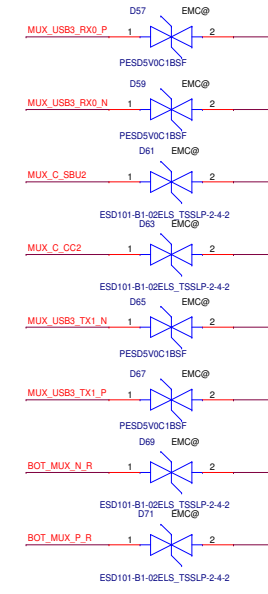
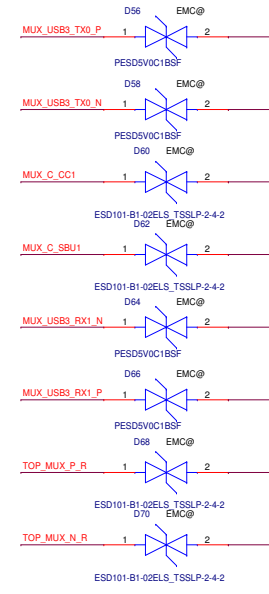
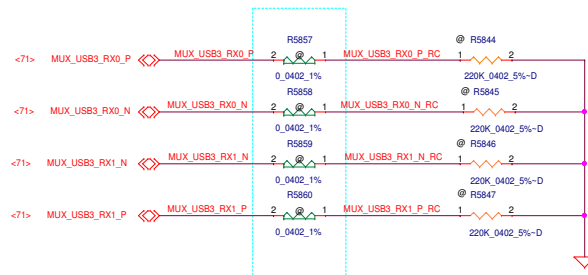
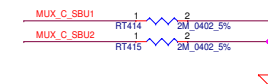
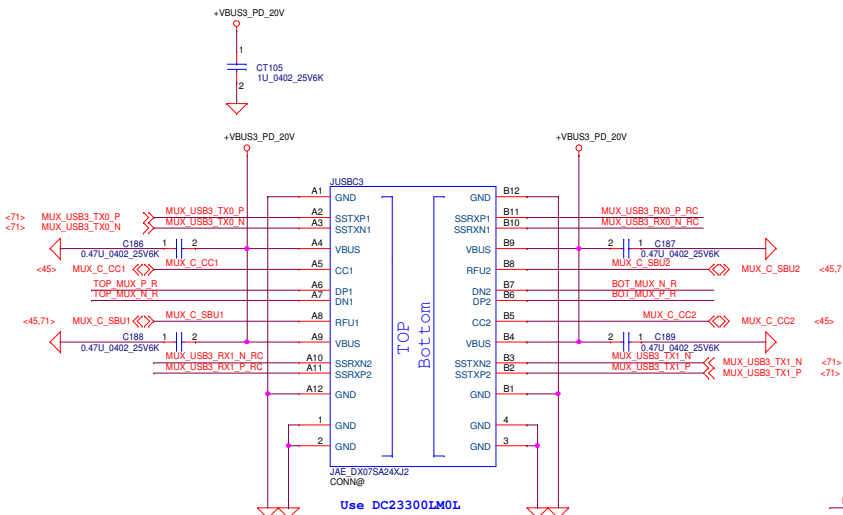
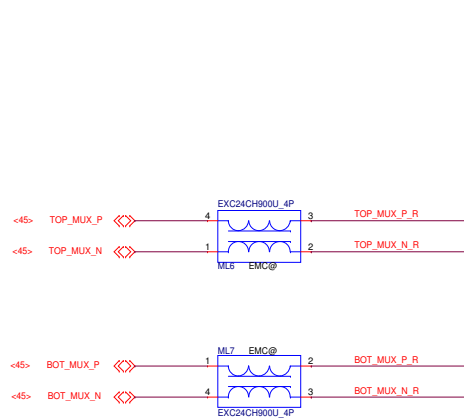
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+VBUS3\_PD\_20V : 5V, 3A



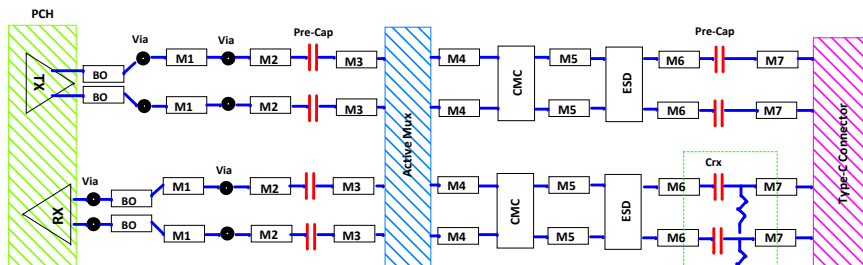


JUSBC1 and JUSBC2 use SP060009R01.





# CNL/CFL Type-C External (Back Panel) Topology with Active Mux



Notes

Crx Cap Value: 297nF to 363nF including tolerance

Rb Resistor Value: 220kΩ ±5%

USB3p1\_Type\_C\_CNUpdate\_CNUpdate\_CNUpdate\_CNUpdate\_CNUpdate .pdf

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P47-PD USB TYPE-C 3			
Size	Document Number	Rev	
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## +3VS\_NGFF: 3.3V, 2A



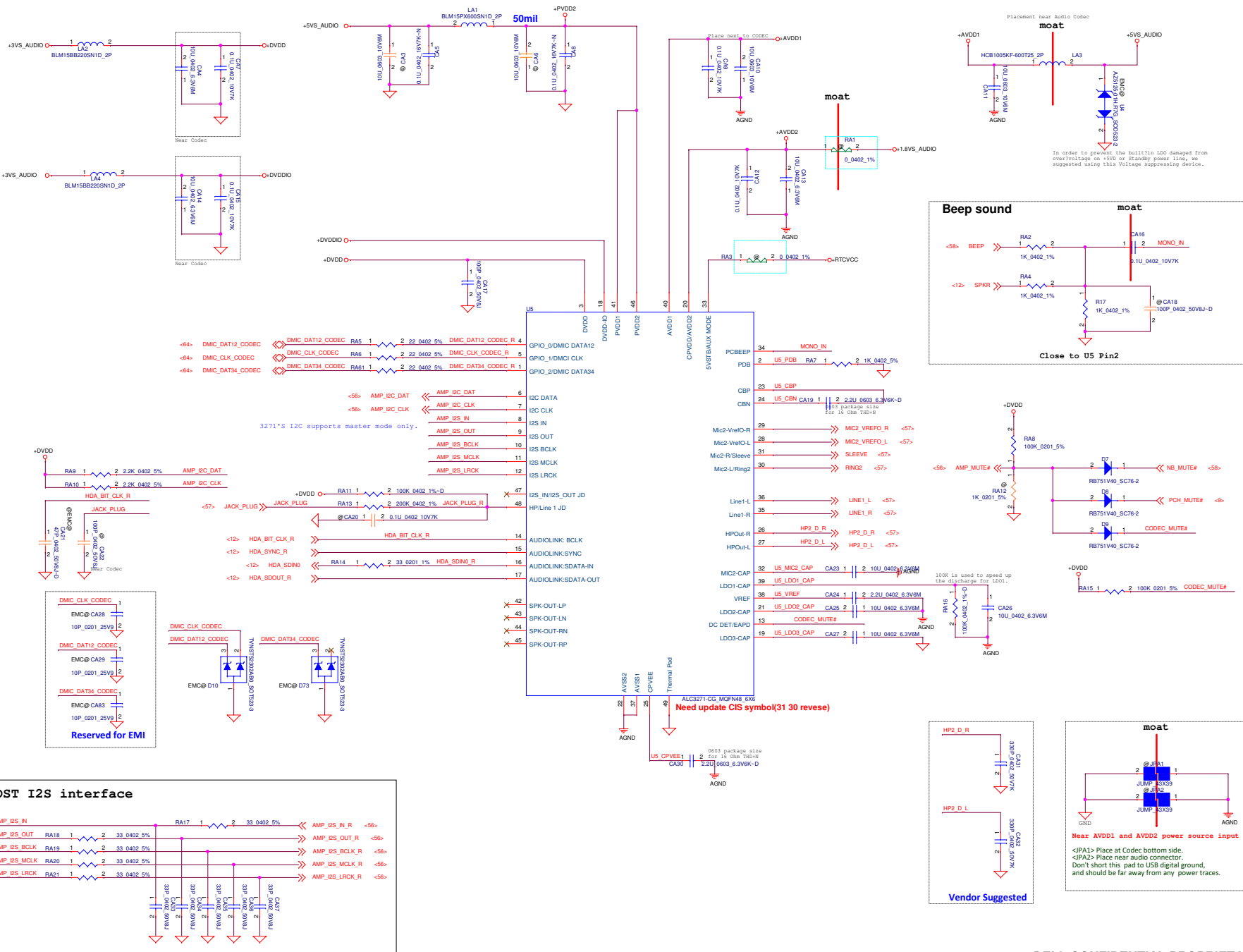


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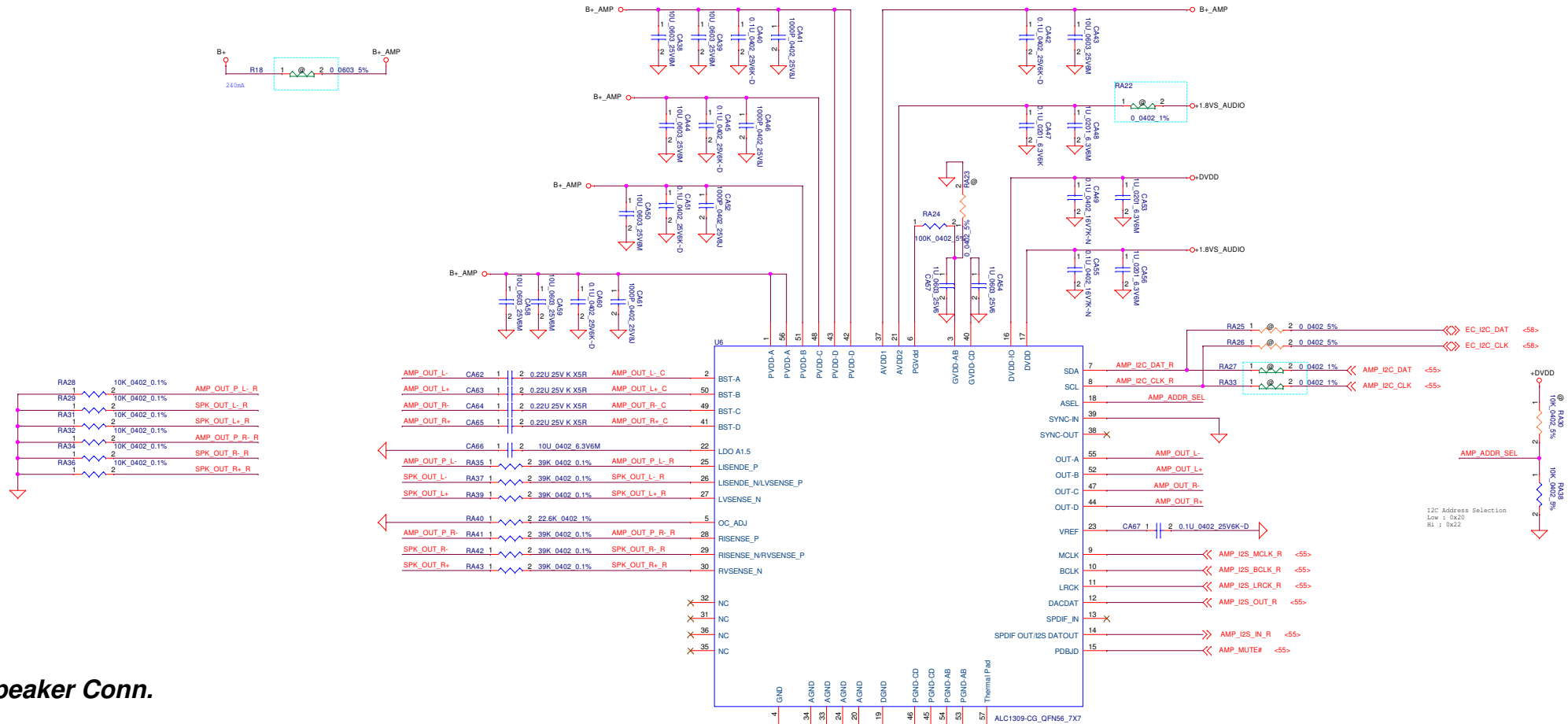
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## HD Audio Codec

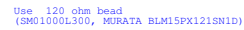


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<p>DATE: 12-19-2018</p>				Ln: H931P	55 of 100

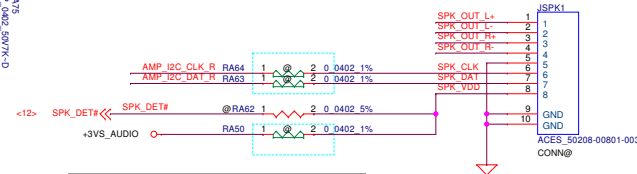
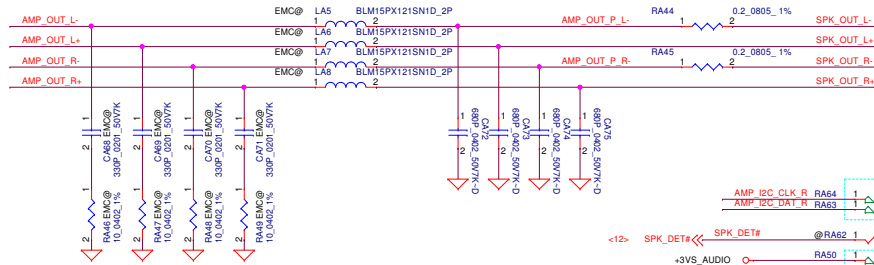
**SMART AMP**



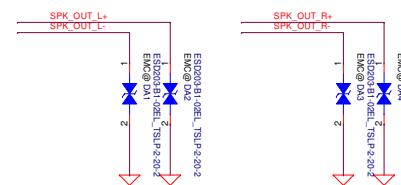
***Int. Speaker Conn.***



40mil = For 4ohm 3W Speaker



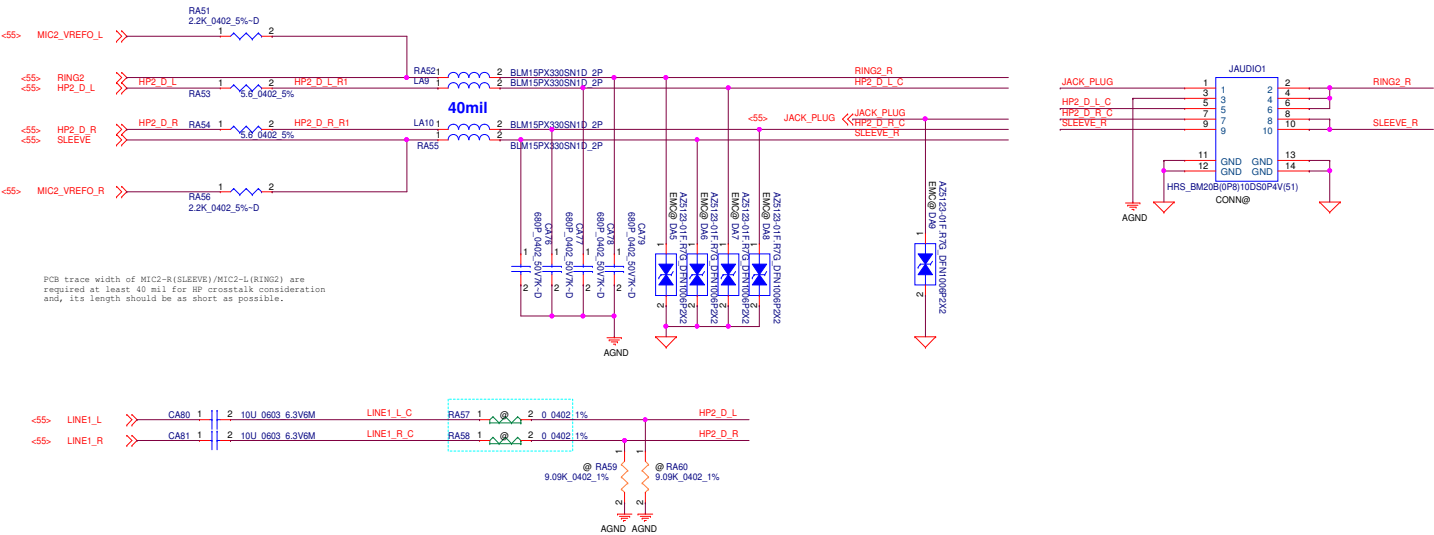
Function	RA50	RA62
EEPROM Speaker	0 ohm	NC
Speaker Detection	10K	0 ohm



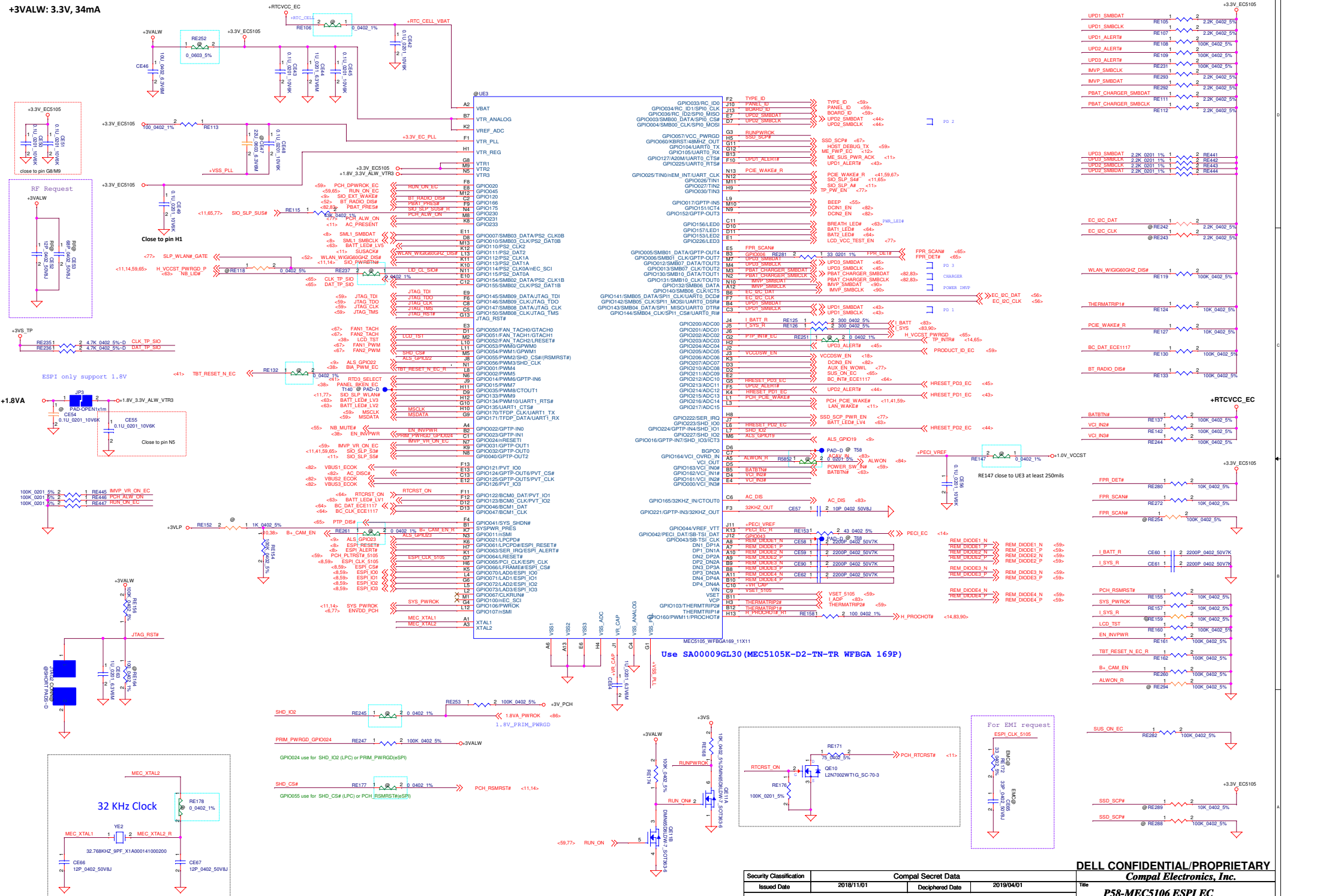
Security Classification	Compal Secret Data		Title	
Issued Date	2018/11/01	Deciphered Date	2019/04/01	<p><b>P56-Smart AMP / Speaker</b></p> <p>Size Document Number: _____ Rev 1.0</p> <p><b>LA-H931P</b></p> <p>Date: <u>12-19-2019</u> (Sheet 58 of 100)</p>
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Universal Audio Jack



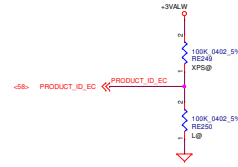
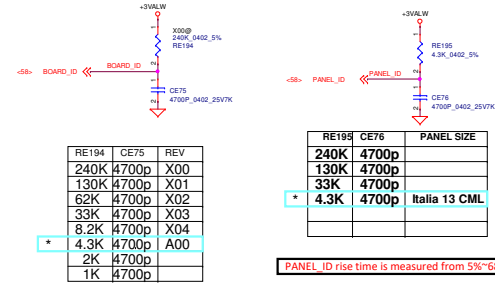
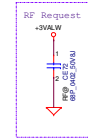
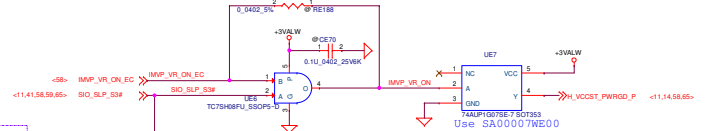
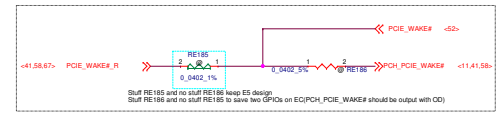
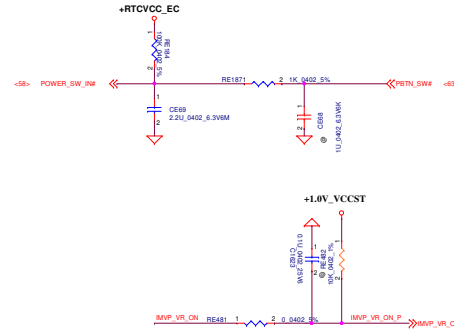
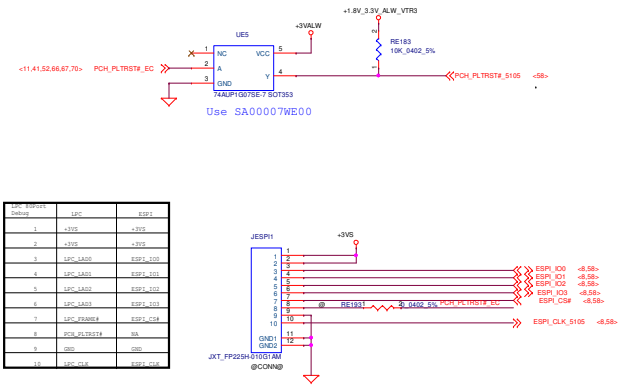
+3VALW: 3.3V, 34mA



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				P58-MEC5106 ESPI EC	1.0
				LA-H931P	
				Date: Friday, June 14, 2019	Sheet 58 of 100

QFN Pinout (Top)	QFN	QFN
1	VDD	VDD
2	VDD	VDD
3	VDD	VDD
4	VDD	VDD
5	VDD	VDD
6	VDD	VDD
7	VDD	VDD
8	VDD	VDD
9	VDD	VDD
10	VDD	VDD



RE249	RE250	REV
@	@	Italia-XPS
@	@	Italia-L

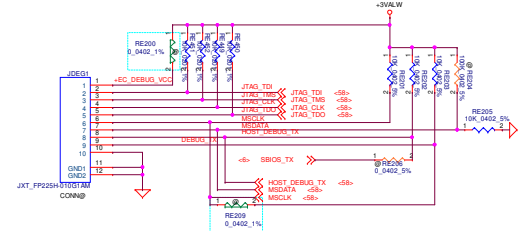
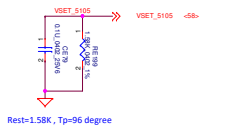
RE196	CE78	REV
* 240K	4700p	U4+2 i5
* 130K	4700p	U2+2
* 62K	4700p	U4+2 i7
* 33K	4700p	U6+2 i7
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

RE194	CE75	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
* 4.3K	4700p	A00
2K	4700p	
1K	4700p	

RE195	CE76	PANEL SIZE
240K	4700p	
130K	4700p	
33K	4700p	
* 4.3K	4700p	Italia 13 CML

PANEL\_ID rise time is measured from 5%~68%

BOARD\_ID rise time is measured from 5%~68%

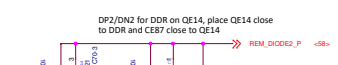


5106 Channel	Location
DP1/DN1	OTP (QE12)
SEN3	DN1a/DP1a Charger (QE20)
TMEM	DP2/DN2 Memory (QE14)
SEN4	DN2a/DP2a Fan (QE21)
TSKN	DP3/DN3 SKIN (QE22)
SEN1	DN3a/DP3a SSD (QE15)
SEN2	DP4/DN4 WLAN (QE19)
	DN4a/DP4a

DP1/DN1 for CPU  
Place CE83 close to the QE12 as possible



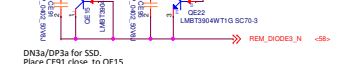
DN1a/DP1a for Charger  
Place QE20 close to chock & CE93 close to the QE20



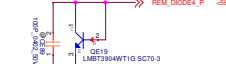
DP2/DN2 for DDR on QE14, place QE14 close to DDR and CE87 close to QE14



DN2a/DP2a for Fan  
Place CE84 close to QE21



DP4/DN4 for WLAN on QE19, place QE19 close to WLAN & QE19 close to CE89.



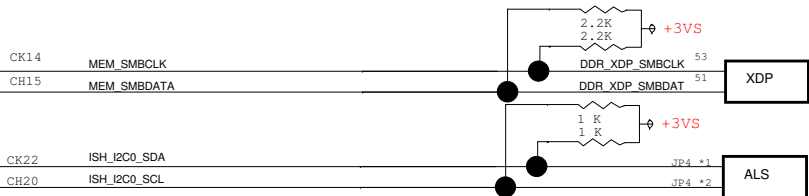
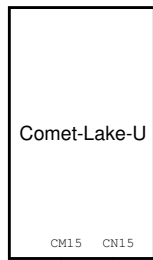
DP3/DN3 for SKIN  
Place CE95 close to the QE22 as possible



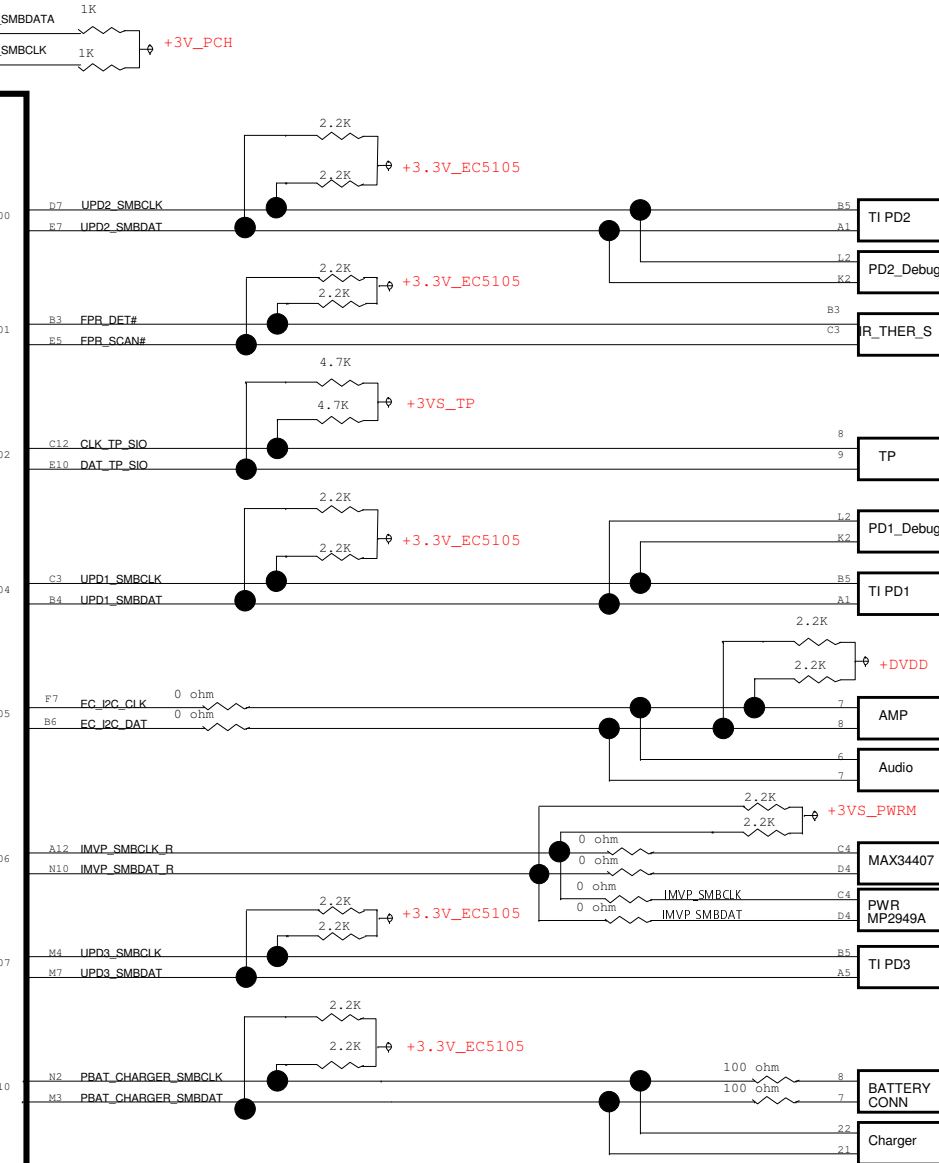
DN3a/DP3a for SSD  
Place CE91 close to QE15







ALS address selection 0x52\_TBD  
Sensor address selection 0x6C\_TBD

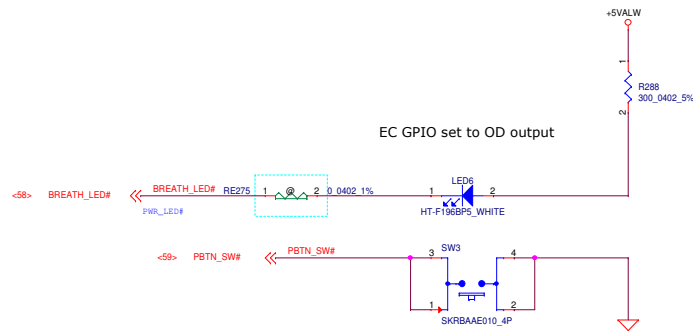


TI PD address selection 0x70\_TBD  
PD\_Debug address selection 0xEC\_TBD  
PD\_Debug address selection 0xEC\_TBD  
TI PD address selection 0x70\_TBD  
I2C address selection L= 0x20H (L= 0x20H ; H= 0x22H)\_TBD  
Battery address selection 0x16\_TBD  
Charger address selection 0x12\_TBD

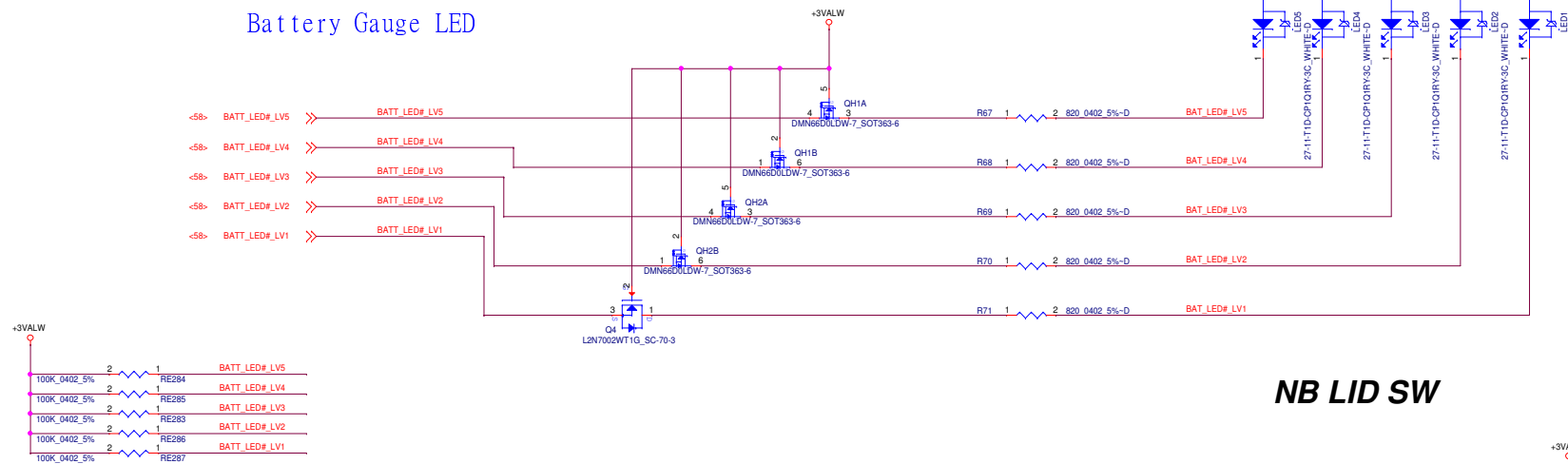


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		Size		Document Number	
		Date:		Wednesday, June 12, 2019	
		Sheet		62 of 100	
		Rev		0.1	
		P062 - Reserve		LA-H931P	

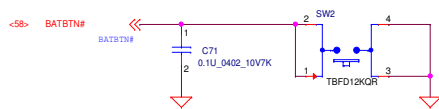
## Power Button +LED



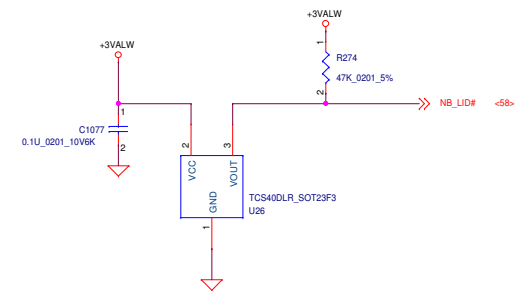
## Battery Gauge LED



## Battery Gauge Button

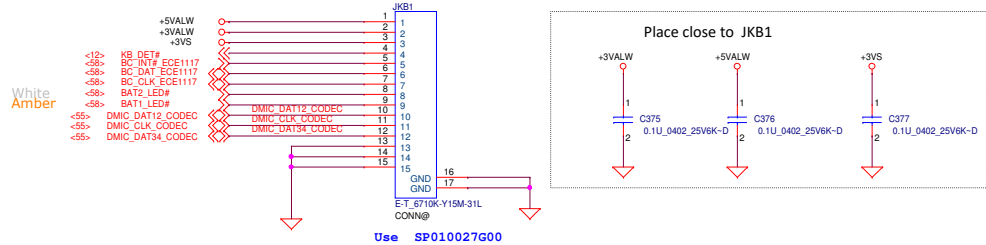


## NB LID SW



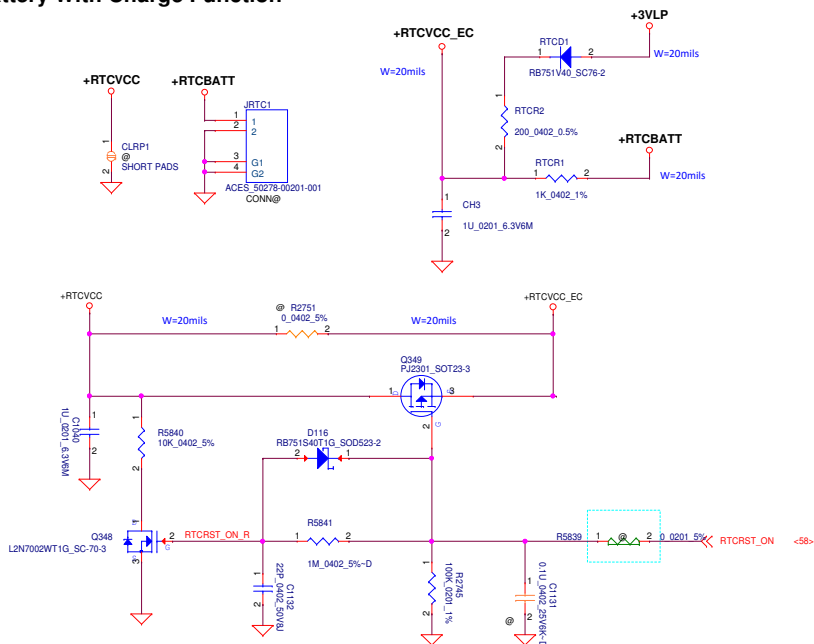
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Issued Date				2018/11/01	Deciphered Date	2019/04/01	Compal Electronics, Inc.
Title				P63-Battery LED / LID			
Size				LA-H931P			
Date:				Wednesday, June 12, 2019			
Sheet				63 of 100			

Keyboard Controller board + DMIC

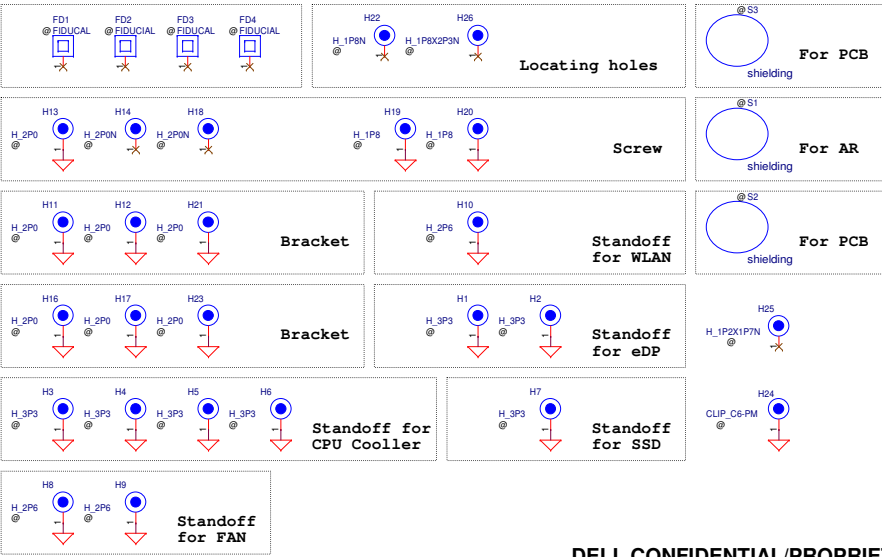


Power Monitor

RTC Battery With Charge Function

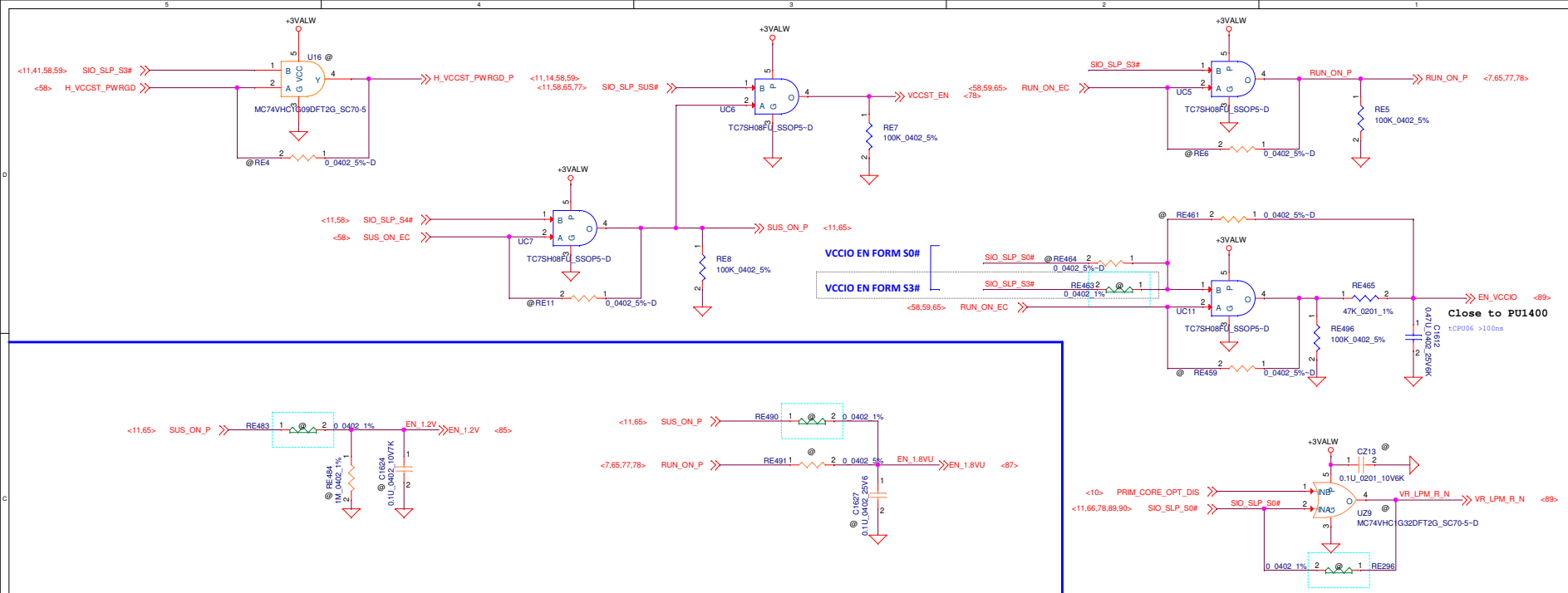


SCREW Hole

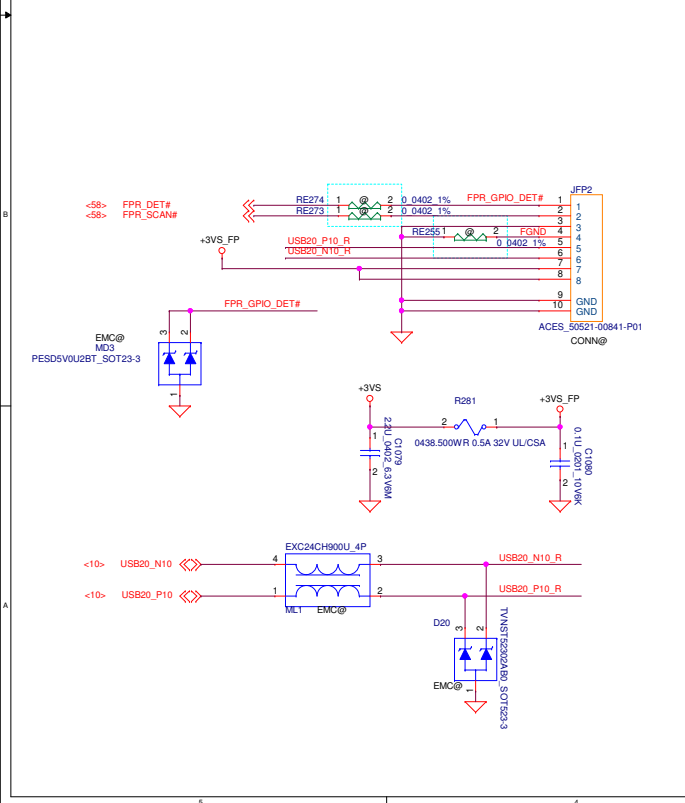


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Issued Date		2018/11/01		Compal Electronics, Inc.	
Deciphered Date		2019/04/01		P64-SCREW/KB/RTC/IR T/PWRM	
Title		Document Number		LA-H931P	
Size		1.0		Rev	
Date: Wednesday, June 12, 2019		Sheet 64 of 100			

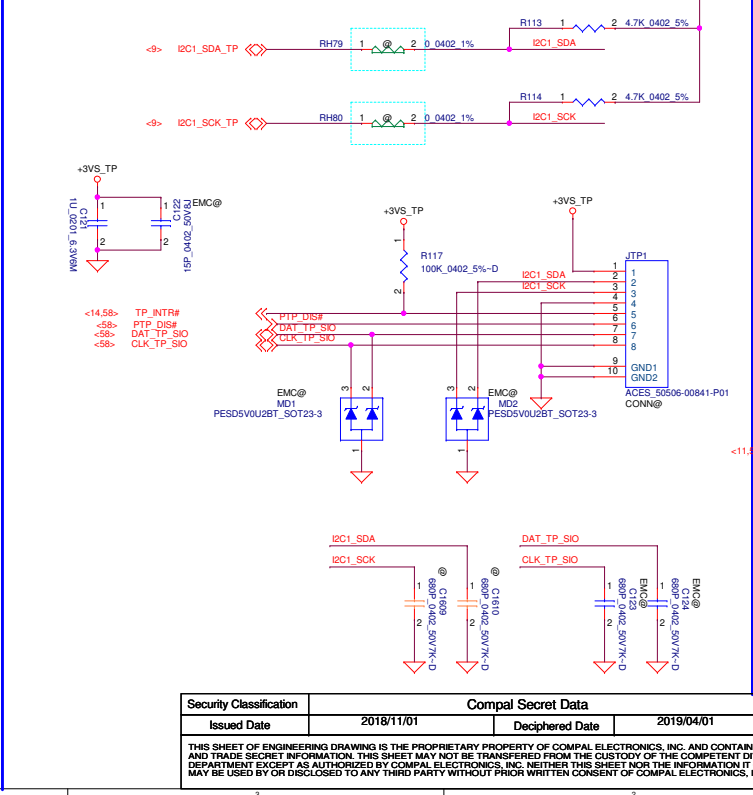




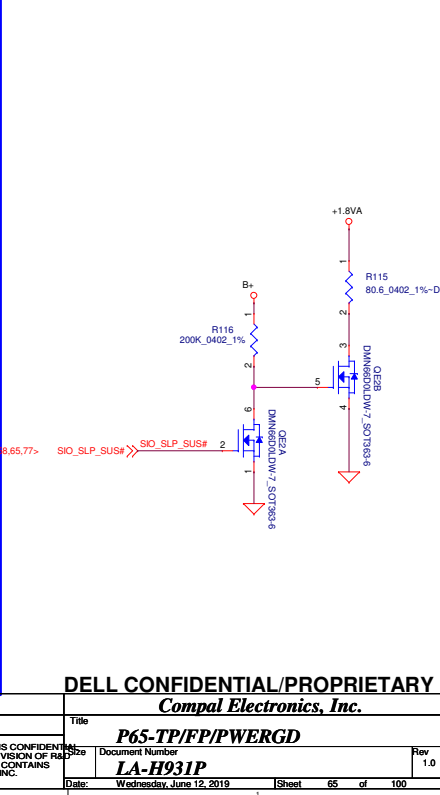
### Fingerprint CONN



### Touchpad CONN



### +1.8VA Discharge



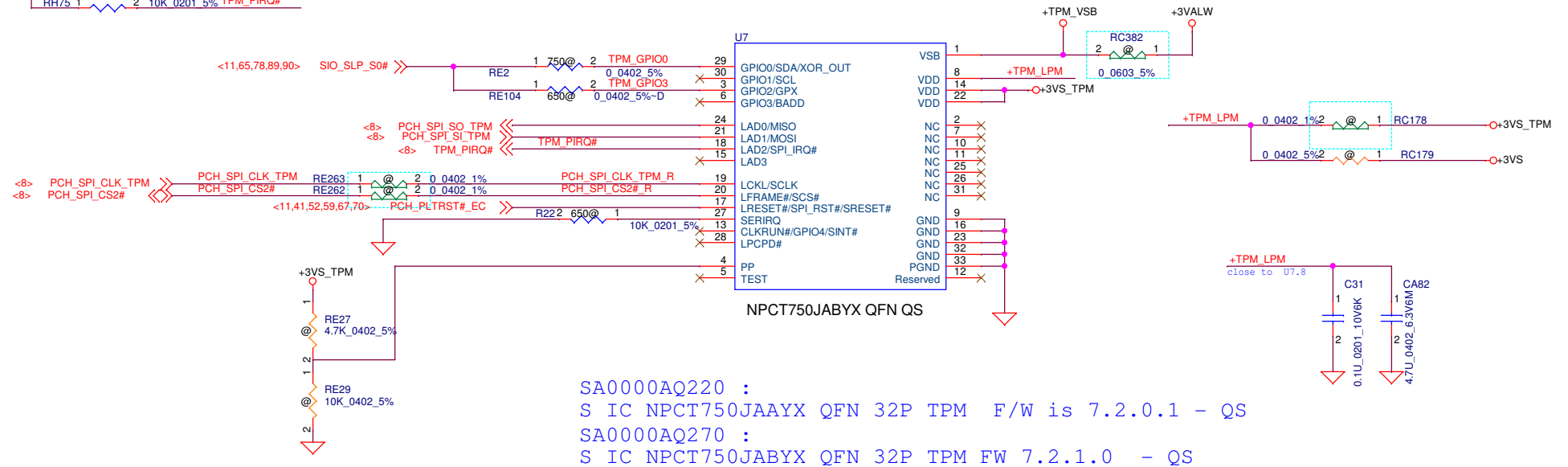
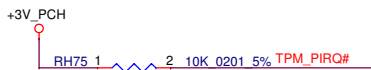
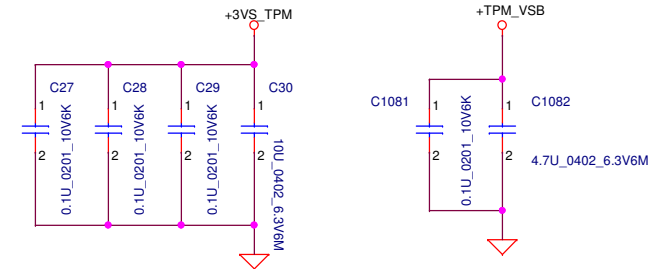
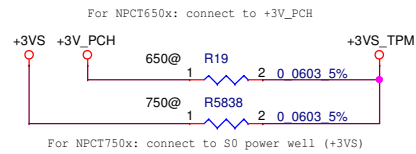
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		LA-H931P		Rev 1.0	
Date: Wednesday, June 12, 2019		Sheet 65 of 100			

## +3V\_PCH: 3.3V, 45mA

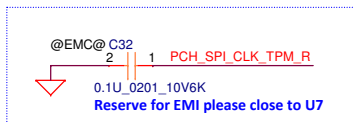
NOTE:  
Follow the SPI topology layout guidelines  
in the relevant Intel Platform Design Guide

# TPM

NOTE:  
Place 0.1 uF capacitors as close as  
possible to the device power pins



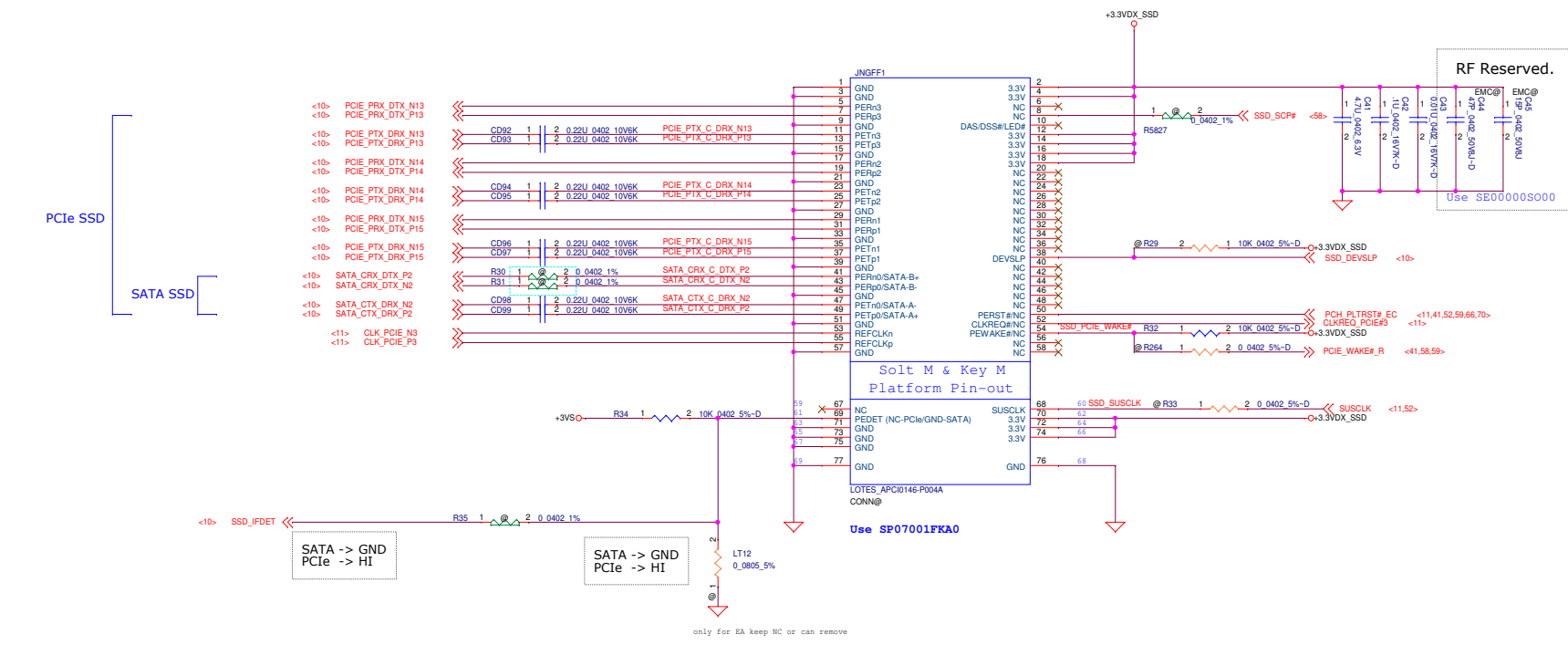
SA0000AQ220 :  
S IC NPCT750JAAYX QFN 32P TPM F/W is 7.2.0.1 - QS  
SA0000AQ270 :  
S IC NPCT750JABYX QFN 32P TPM FW 7.2.1.0 - QS



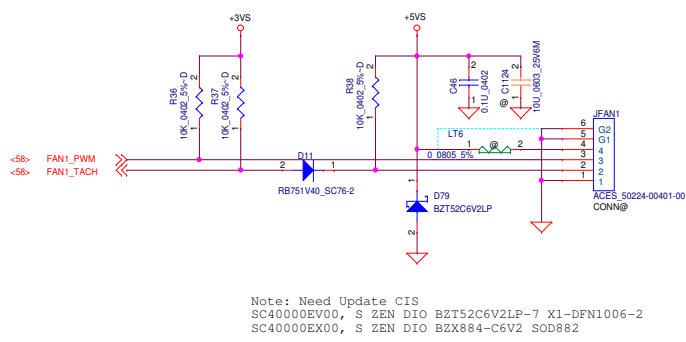
- Pin14&Pin22 (+3VS\_TPM):  
For NPCT650x: connect to same power well with host SPI interface (it should be +3V\_PCH)  
For NPCT750x: connect to S0 power well (+3VS)
- Pin27:  
For NPCT650x: pop R22  
For NPCT750x: de-pop R22
- SLP\_S0# connection:  
For NPCT650x: pop RE104, de-pop RE2  
For NPCT750x: pop RE2, de-pop RE104
- RC180 can be just deleted for both NPCT650x and NPCT750x
- TPM\_PIRQ# is recommended that pull-up to same GPIO power well at host side

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2018/11/01		2019/04/01		Title	
2019/04/01		2019/04/01		P66-TPM	
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M.2 Slot-C Key-M (SSD)

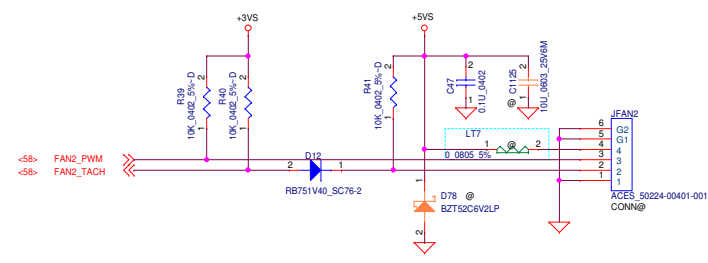


FAN 1



Note: Need Update CIS  
SC40000EV00, S ZEN DIO BZT52C6V2LP-7 X1-DFN1006-2  
SC40000EV00, S ZEN DIO BZX884-C6V2 SOD882

FAN 2



Note: Need Update CIS  
SC40000EX00, S ZEN DIO BZX884-C6V2 SOD882  
SC40000EV00, S ZEN DIO BZT52C6V2LP-7 X1-DFN1006-2

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				Document Number	
				LA-H931P	
				Rev 1.0	
				Date: Wednesday, June 12, 2019	
				Sheet 67 of 100	



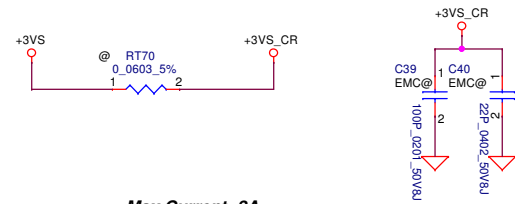
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Issued Date	2018/11/01	Deciphered Date	2019/04/01	Title	P68-Reserved
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				Date:	Wednesday, June 12, 2019
				Sheet	68 of 100
				Rev	0.1
				LA-H931P	



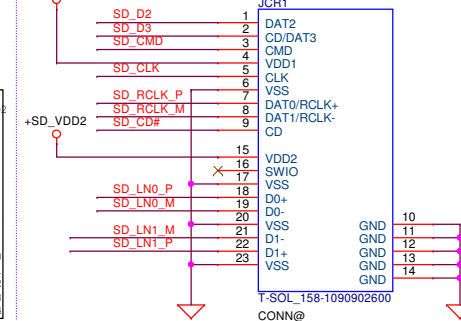
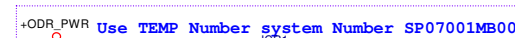
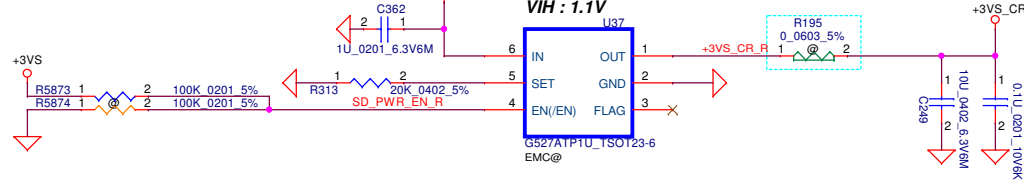
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				Sheet	69 of 100
				Rev	0.1
				LA-H931P	

## Card Reader

**+3VS\_CR: 3.3V, 1.575A**

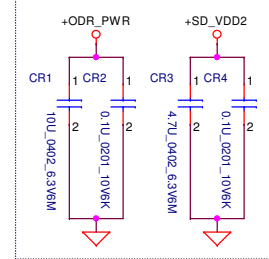


+3VS\_CR

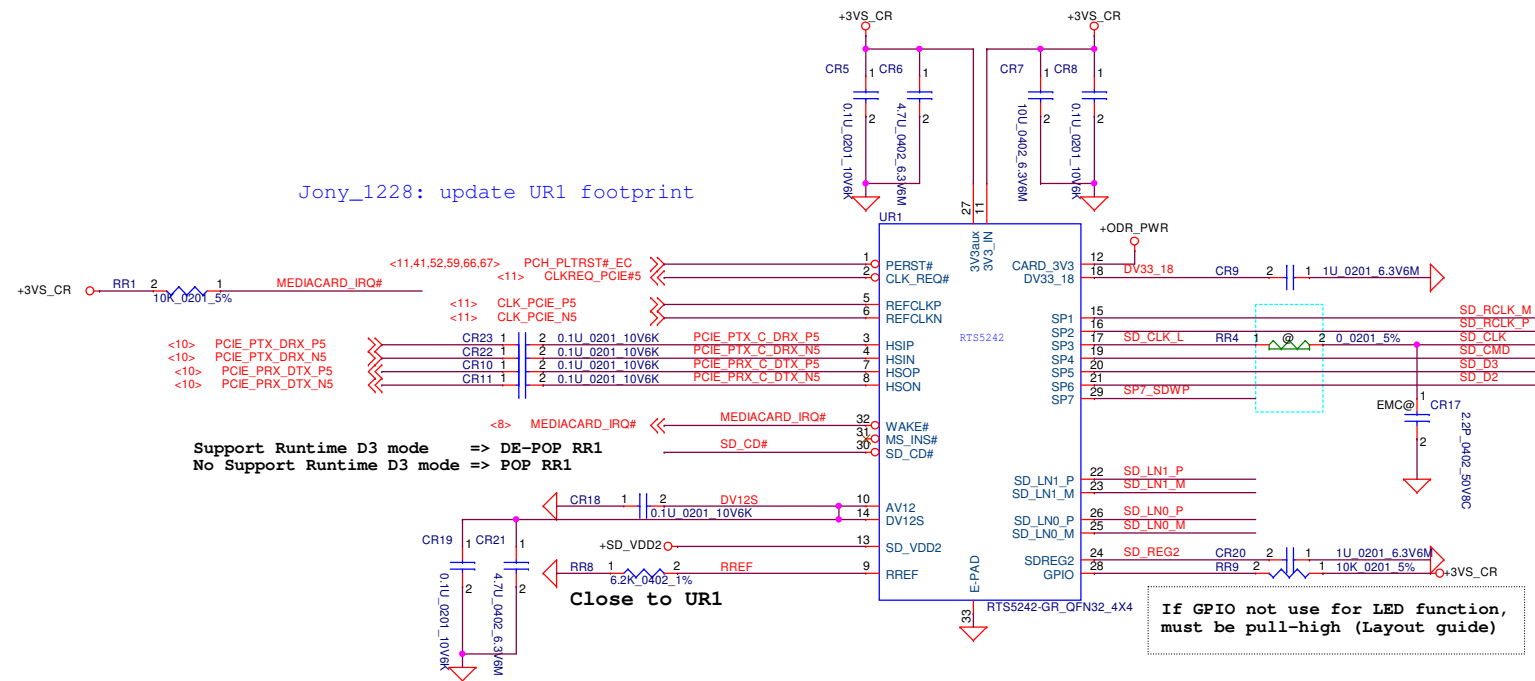


```
Tom0114:wait CIS symbol
TAISOL 158-1160902600
VDD1=ODR_PWR=3.3V
VDD2=SD_VDD2=1.8V
changed footprint & CPN
```

Close to JCR1



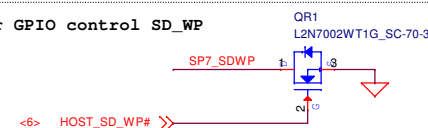
Jony\_1228: update UR1 footprint



- 1) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
- 2) Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
  - Bulk capacitor for Card\_3V3 place closed to flash card socket.
  - Bulk capacitor for 3V3\_IN / 3V3aux / DV12S place closed to RTS5242 chip.
- 3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.

If GPIO not use for LED function,  
must be pull-high (Layout guide)

```
For GPIO control SD_WP
```



<6> HOST\_SD\_WP#

+3VS\_CR  
RR10  
@  
10K\_0201\_5%  
SP7 SDWP

**DELL CONFIDENTIAL/PROPRIETARY**

**Compal Electronics, Inc.**

**P70-Card Reader - RT5242**

Document Number  
**LA-H931P**

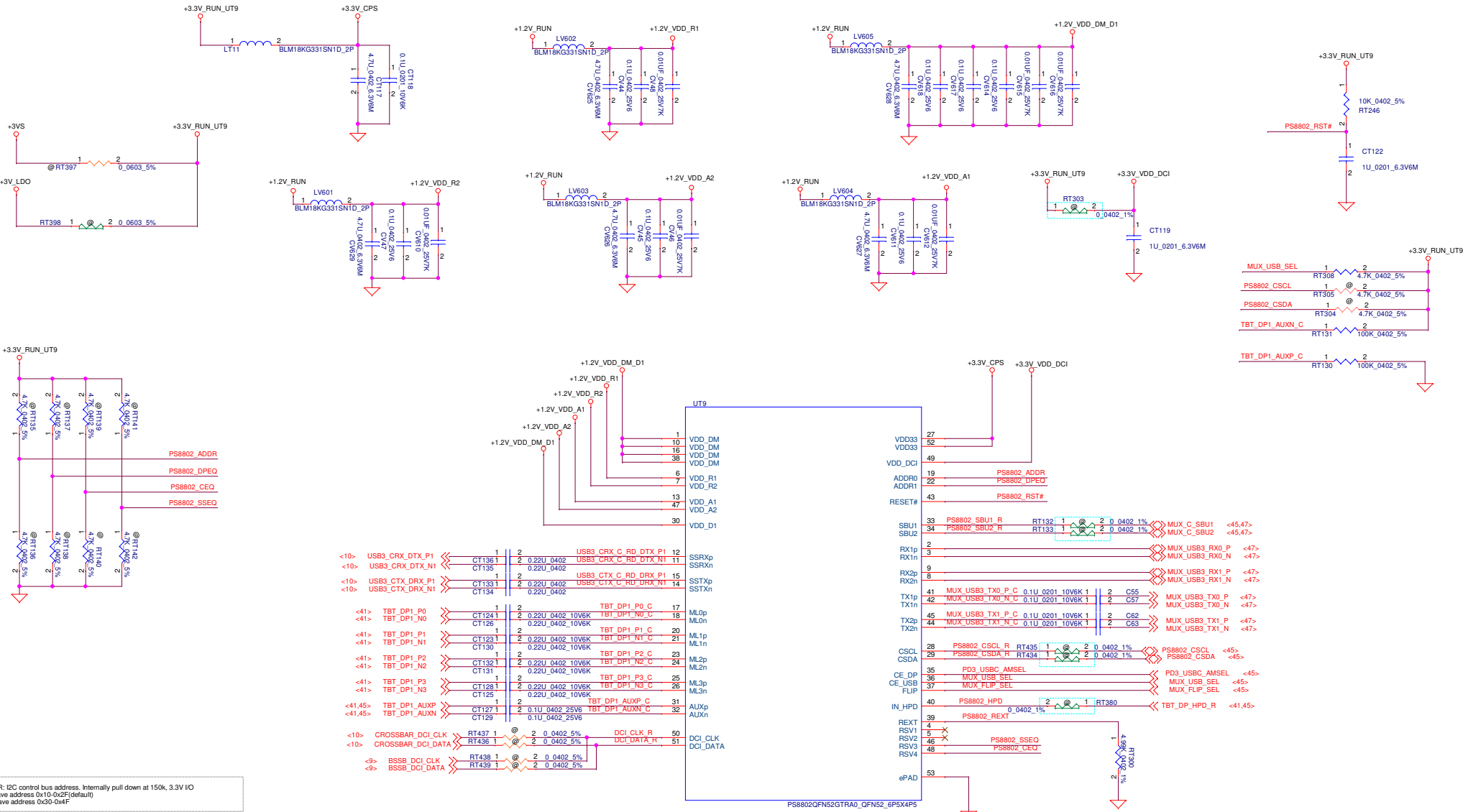
Rev	1.0
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Date: Friday, June 14, 2019

Sheet 70 of 100

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Issued Date	2018/11/01	Deciphered Date	2019/04/01
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+3.3V\_RUN\_UT9: 3.3V, 23mA  
+1.2V\_RUN: 1.2V, 393mA



ADDR: I2C control bus address. Internally pull down at 150k, 3.3V I/O  
L: Slave address 0x10-0x2F (default)  
H: Slave address 0x30-0x4F

DPEQ:DP Receiver equalization setting; Internally pull down at 150k, 3.3V I/O  
L: Compensation for channel loss up to 12dB (Default)  
H: Compensation for channel loss up to 18dB

CEQ: USB Type-C connector facing Rx channel receiver equalization setting;  
Internally pull down at 150k, 3.3V I/O  
L: Compensation for channel loss up to 16dB (Default)  
H: Compensation for channel loss up to 18dB

SSEQ: USB Host facing Rx channel receiver equalization setting;  
Internally pull down at 150k, 3.3V I/O  
L: Compensation for channel loss up to 12dB (Default)  
H: Compensation for channel loss up to 18dB



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				Size	Document Number <b>LA-H931P</b>
				Date	Wednesday, June 12, 2019
				Sheet	72 of 100
				Rev	0.1

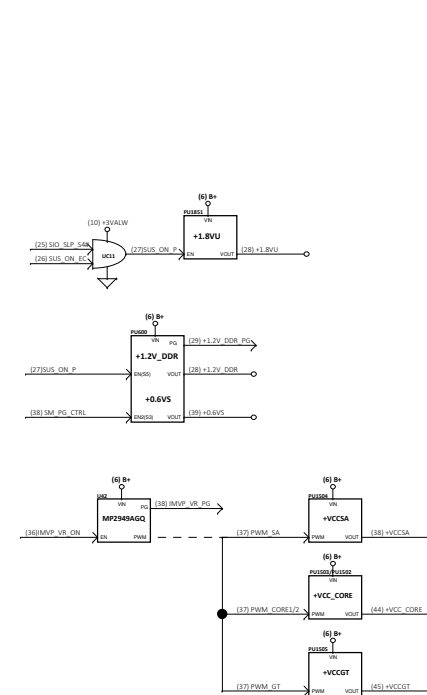




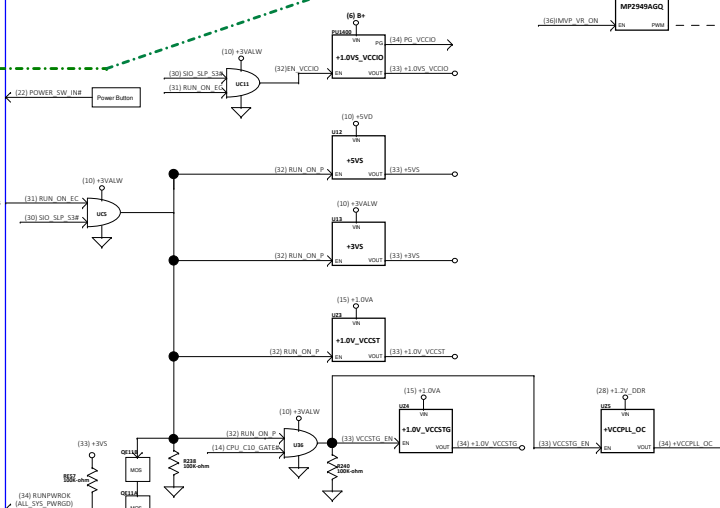
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Issued Date		2018/11/01		Compal Electronics, Inc.		
Deciphered Date		2019/04/01		Title		
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				LA-H931P		Rev
				0.1		
Date:	Wednesday, June 12, 2019			Sheet	73 of 100	



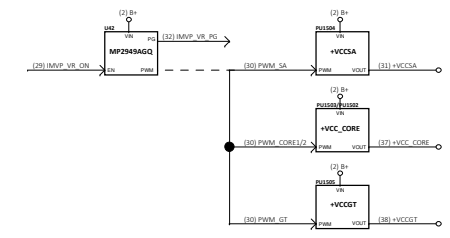
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				Date:	Wednesday, June 12, 2019
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(14) CPU\_C10\_GATE# CPU\_C10\_GATE#

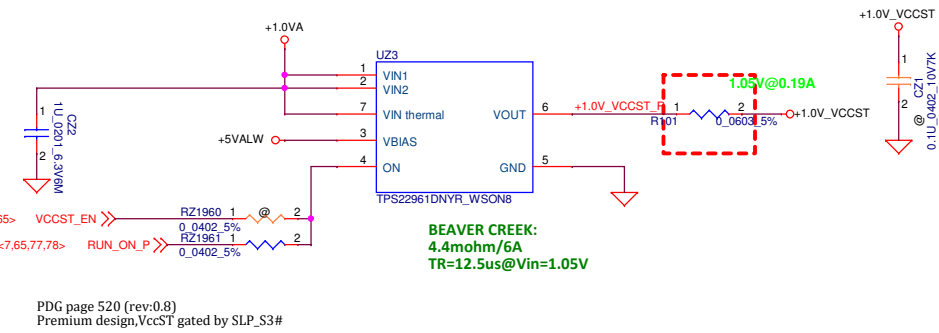


**S5 to S0  
(22)~(42)**

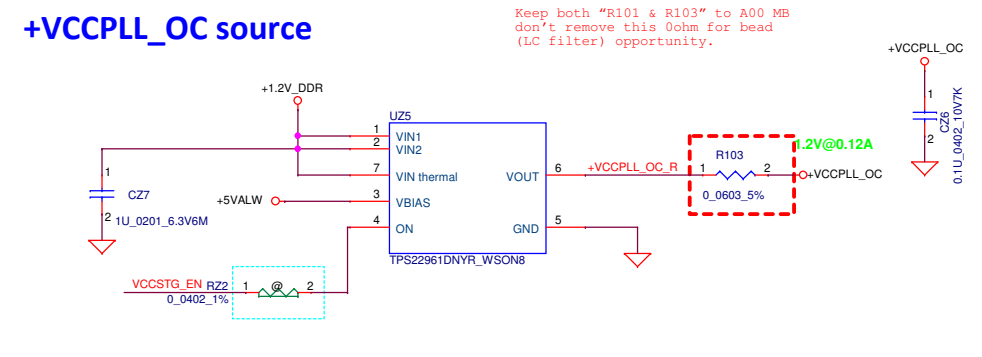




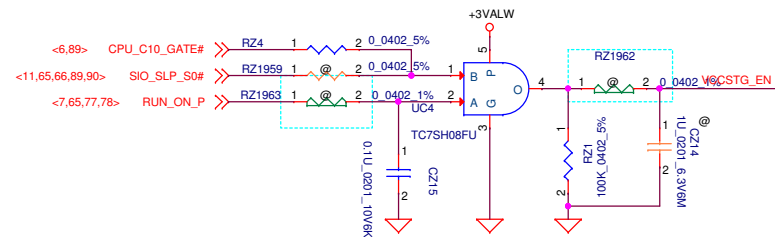
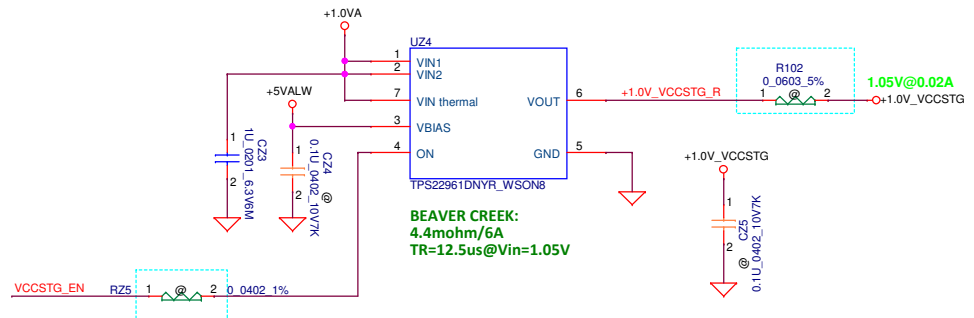
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## +VCCPLL\_OC source

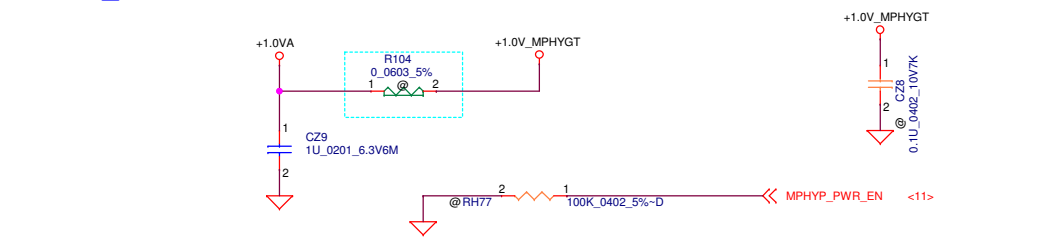


## +1.0V\_VCCSTG source



	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

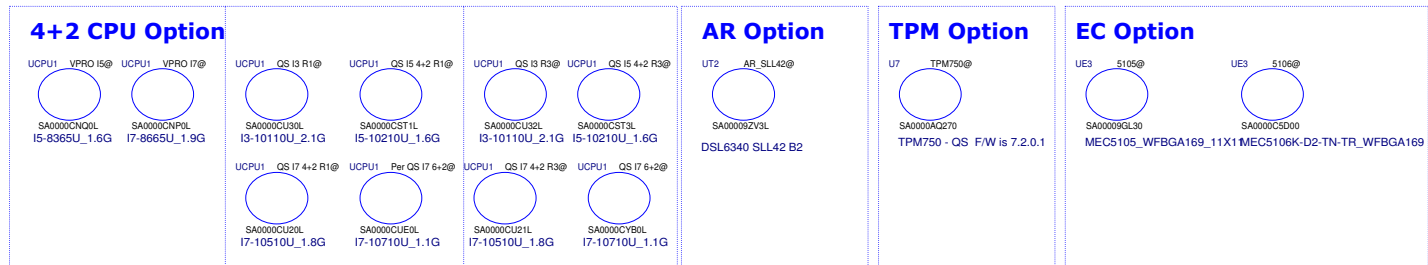
## +1.0V\_MPHYGT source



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				Deciphered Date				P78-DC/DC Interface 2			
				2019/04/01				Document Number			
								LA-H931P			
								Date			
								Wednesday, June 12, 2019			
								Sheet			
								78 of 100			

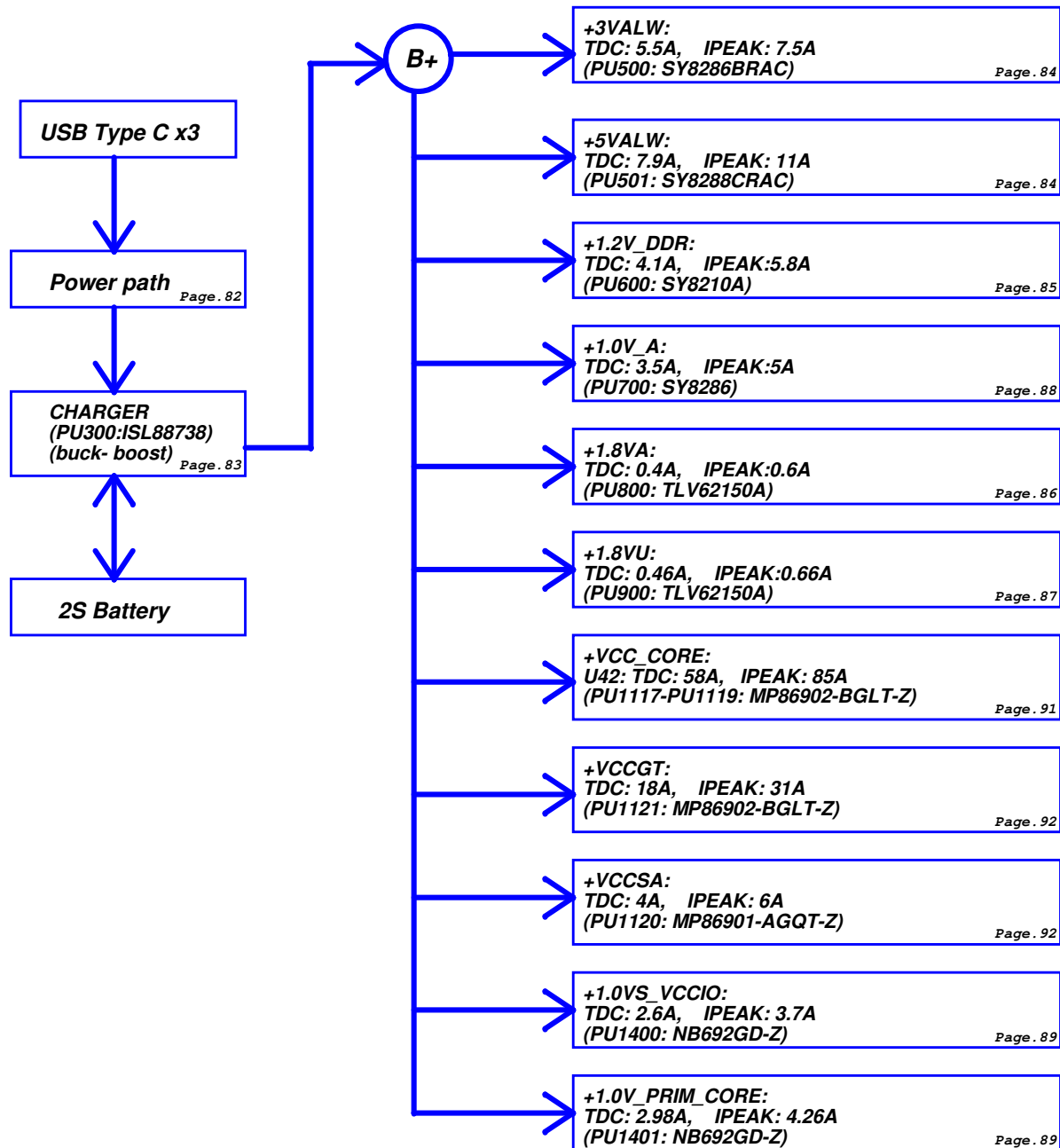


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				Sheet	79 of 100
				Rev	0.1
				LA-H931P	

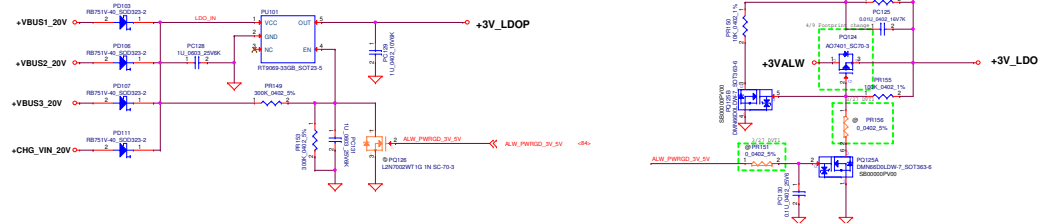
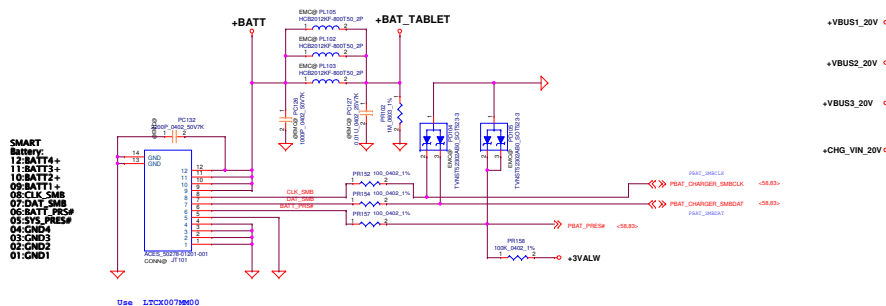
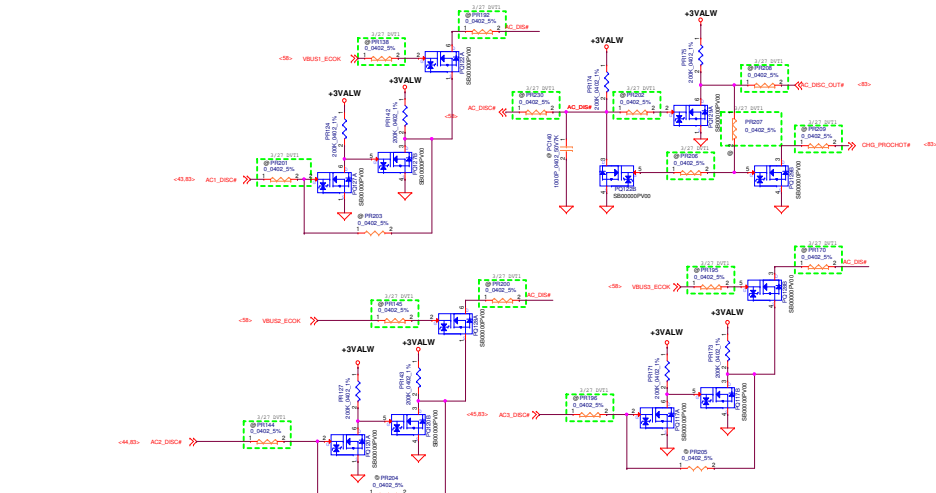
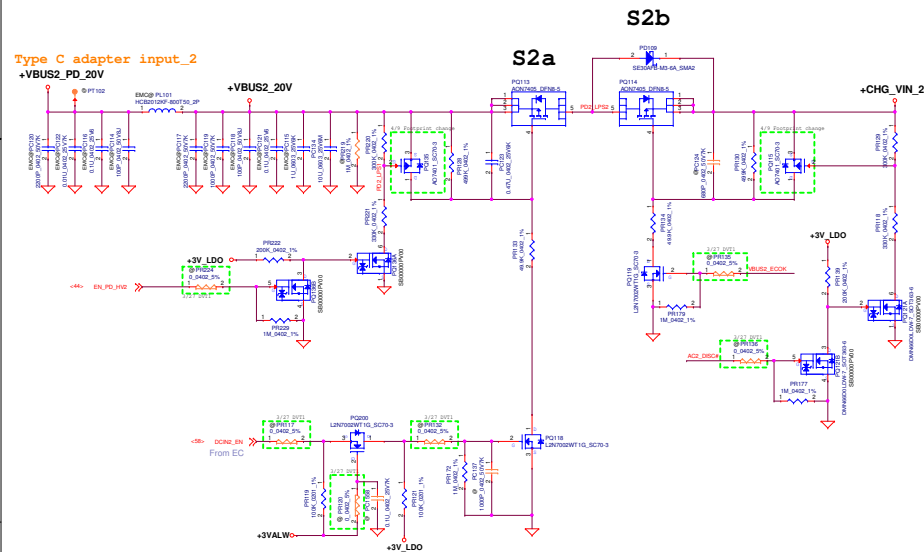
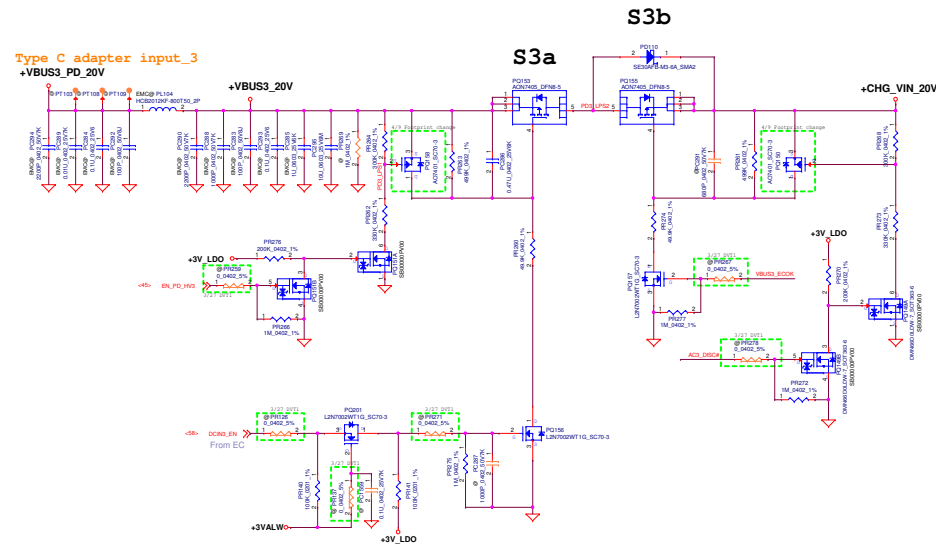
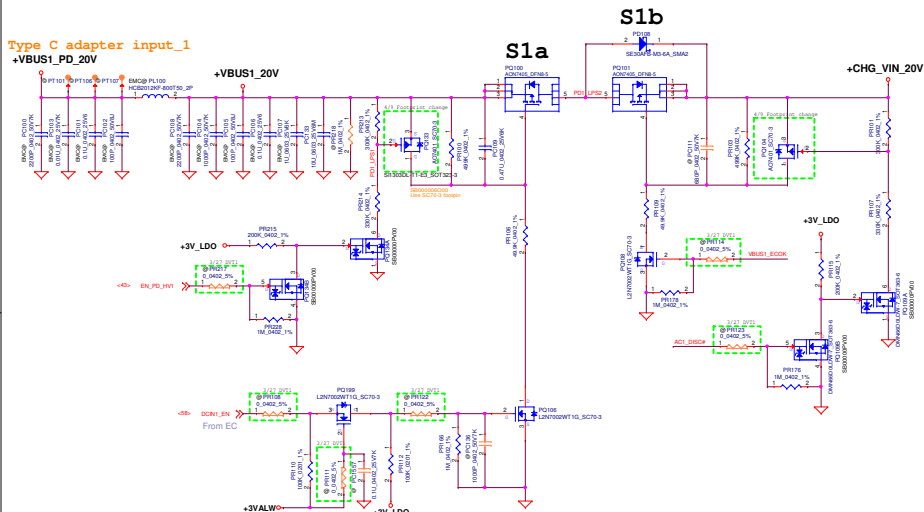


DRAM Option					DRAM Config Option				
Samsung 4G/2133	UD41 S4G_2133@  SA0000BTE1L SA0000BTE1L K4E8E324EB-EGCG	UD42 S4G_2133@  SA0000BTE1L SA0000BTE1L K4E8E324EB-EGCG	UD43 S4G_2133@  SA0000BTE1L SA0000BTE1L K4E8E324EB-EGCG	UD44 S4G_2133@  SA0000BTE1L SA0000BTE1L K4E8E324EB-EGCG	MEM_CONFIG0 RH52 S4G_2133@  SD028100280 10K_0402_5%-D	MEM_CONFIG1 RH54 S4G_2133@  SD028100280 10K_0402_5%-D	MEM_CONFIG2 RH56 S4G_2133@  SD028100280 10K_0402_5%-D	MEM_CONFIG3 RH57 S4G_2133@  SD028100280 10K_0402_5%-D	MEM_CONFIG4 RH59 S4G_2133@  SD028100280 10K_0402_5%-D
	UD41 S8G_2133@  SA0000AZT2L SA0000AZT2L K4E6E304EC-EGCG	UD42 S8G_2133@  SA0000AZT2L SA0000AZT2L K4E6E304EC-EGCG	UD43 S8G_2133@  SA0000AZT2L SA0000AZT2L K4E6E304EC-EGCG	UD44 S8G_2133@  SA0000AZT2L SA0000AZT2L K4E6E304EC-EGCG	RH51 S8G_2133@  SD028100280 10K_0402_5%-D	RH54 S8G_2133@  SD028100280 10K_0402_5%-D	RH56 S8G_2133@  SD028100280 10K_0402_5%-D	RH57 S8G_2133@  SD028100280 10K_0402_5%-D	RH59 S8G_2133@  SD028100280 10K_0402_5%-D
	UD41 S16G_2133@  SA00008VV3L SA00008VV3L K4E8E304EC-EGCG	UD42 S16G_2133@  SA00008VV3L SA00008VV3L K4E8E304EC-EGCG	UD43 S16G_2133@  SA00008VV3L SA00008VV3L K4E8E304EC-EGCG	UD44 S16G_2133@  SA00008VV3L SA00008VV3L K4E8E304EC-EGCG	RH52 S16G_2133@  SD028100280 10K_0402_5%-D	RH53 S16G_2133@  SD028100280 10K_0402_5%-D	RH56 S16G_2133@  SD028100280 10K_0402_5%-D	RH57 S16G_2133@  SD028100280 10K_0402_5%-D	RH59 S16G_2133@  SD028100280 10K_0402_5%-D
	UD41 H4G_2133@  SA0000AZR1L SA0000AZR1L H9CCNNN8GTALAR-NVD	UD42 H4G_2133@  SA0000AZR1L SA0000AZR1L H9CCNNN8GTALAR-NVD	UD43 H4G_2133@  SA0000AZR1L SA0000AZR1L H9CCNNN8GTALAR-NVD	UD44 H4G_2133@  SA0000AZR1L SA0000AZR1L H9CCNNN8GTALAR-NVD	RH51 H4G_2133@  SD028100280 10K_0402_5%-D	RH54 H4G_2133@  SD028100280 10K_0402_5%-D	RH55 H4G_2133@  SD028100280 10K_0402_5%-D	RH58 H4G_2133@  SD028100280 10K_0402_5%-D	RH59 H4G_2133@  SD028100280 10K_0402_5%-D
UD41 H8G_2133@  SA0000ALP1L SA0000ALP1L H9CCNNNBJTALAR-NVD	UD42 H8G_2133@  SA0000ALP1L SA0000ALP1L H9CCNNNBJTALAR-NVD	UD43 H8G_2133@  SA0000ALP1L SA0000ALP1L H9CCNNNBJTALAR-NVD	UD44 H8G_2133@  SA0000ALP1L SA0000ALP1L H9CCNNNBJTALAR-NVD	RH52 H8G_2133@  SD028100280 10K_0402_5%-D	RH53 H8G_2133@  SD028100280 10K_0402_5%-D	RH55 H8G_2133@  SD028100280 10K_0402_5%-D	RH58 H8G_2133@  SD028100280 10K_0402_5%-D	RH59 H8G_2133@  SD028100280 10K_0402_5%-D	
UD41 H16G_2133@  SA00009ZL1L SA00009ZL1L H9CCNNNCLGALAR-NVD	UD42 H16G_2133@  SA00009ZL1L SA00009ZL1L H9CCNNNCLGALAR-NVD	UD43 H16G_2133@  SA00009ZL1L SA00009ZL1L H9CCNNNCLGALAR-NVD	UD44 H16G_2133@  SA00009ZL1L SA00009ZL1L H9CCNNNCLGALAR-NVD	RH51 H16G_2133@  SD028100280 10K_0402_5%-D	RH53 H16G_2133@  SD028100280 10K_0402_5%-D	RH55 H16G_2133@  SD028100280 10K_0402_5%-D	RH58 H16G_2133@  SD028100280 10K_0402_5%-D	RH59 H16G_2133@  SD028100280 10K_0402_5%-D	



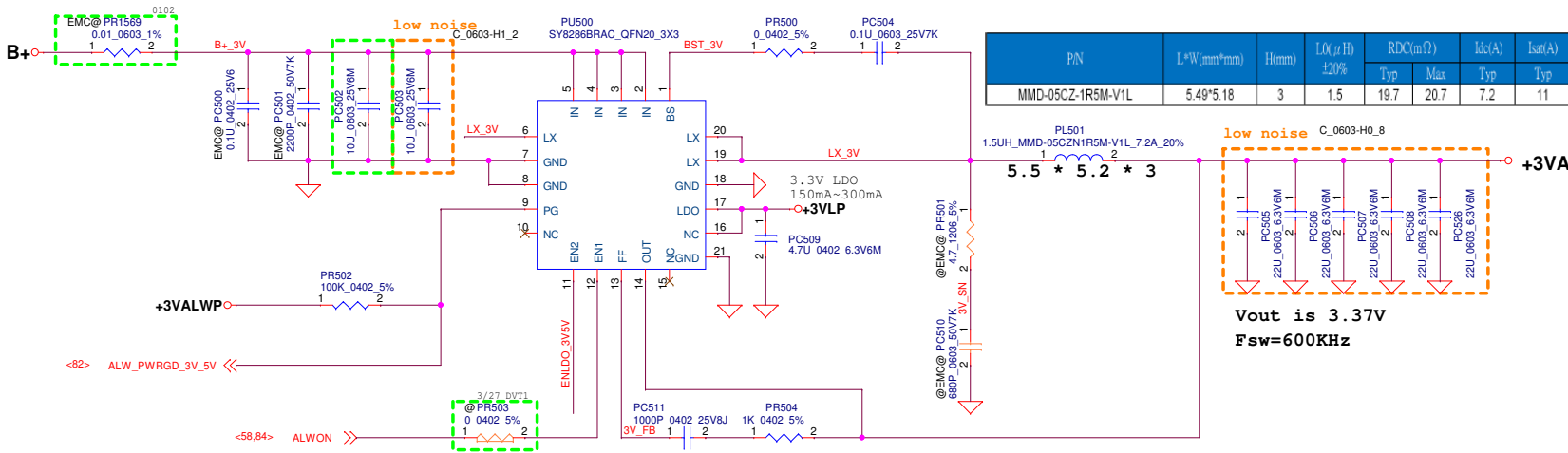


Function feild:  
Power Path(37.1), EMC Part(47.1)



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+3VALWP

© PJP500  
JUMP 43X118

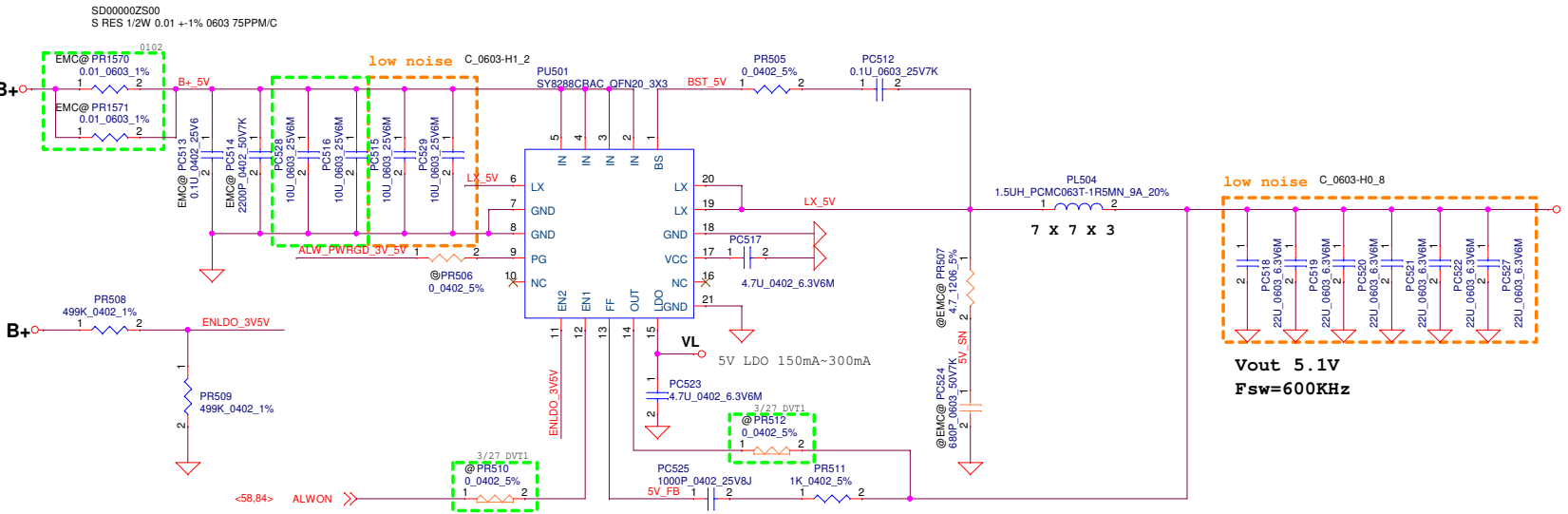
**3VALWP**  
TDC 5.2A  
Peak Current 7.5A  
OCP Current 8.0A (fix)

**Non AR**  
**3VALWP**  
TDC 5.5A  
Peak Current 7.5A  
OCP Current 8.0A (fix)

+5VALWP

© PJP501  
JUMP 43X118

**5VALWP**  
TDC 7.9A  
Peak Current 11.0A  
OCP Current 13.0A



3V/5V controller(35.1), Support component(35.2)

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								Size	Document Number	Rev			
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	LPM	VID1	VID0	Vout
	0	X	X	0 (LPM)
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

**VCCIO**  
TDC 2.6A  
Peak Current 3.7 A  
OCP Current 7.6 A Fix by IC  
MIN:7A  
MAX:8.5A  
Frequency:750KHz

+1.0VS\_VCCIO

+1.0VS\_VCCIO

V <sub>OUT</sub> (V)	R <sub>Mode</sub> (Ω)
VCCIO	0
PRIMCORE	Float
EDRAM/EOPIO/V1.0A	100K
Others-1.8V/2.5V	150K
Others-3.3V	150K

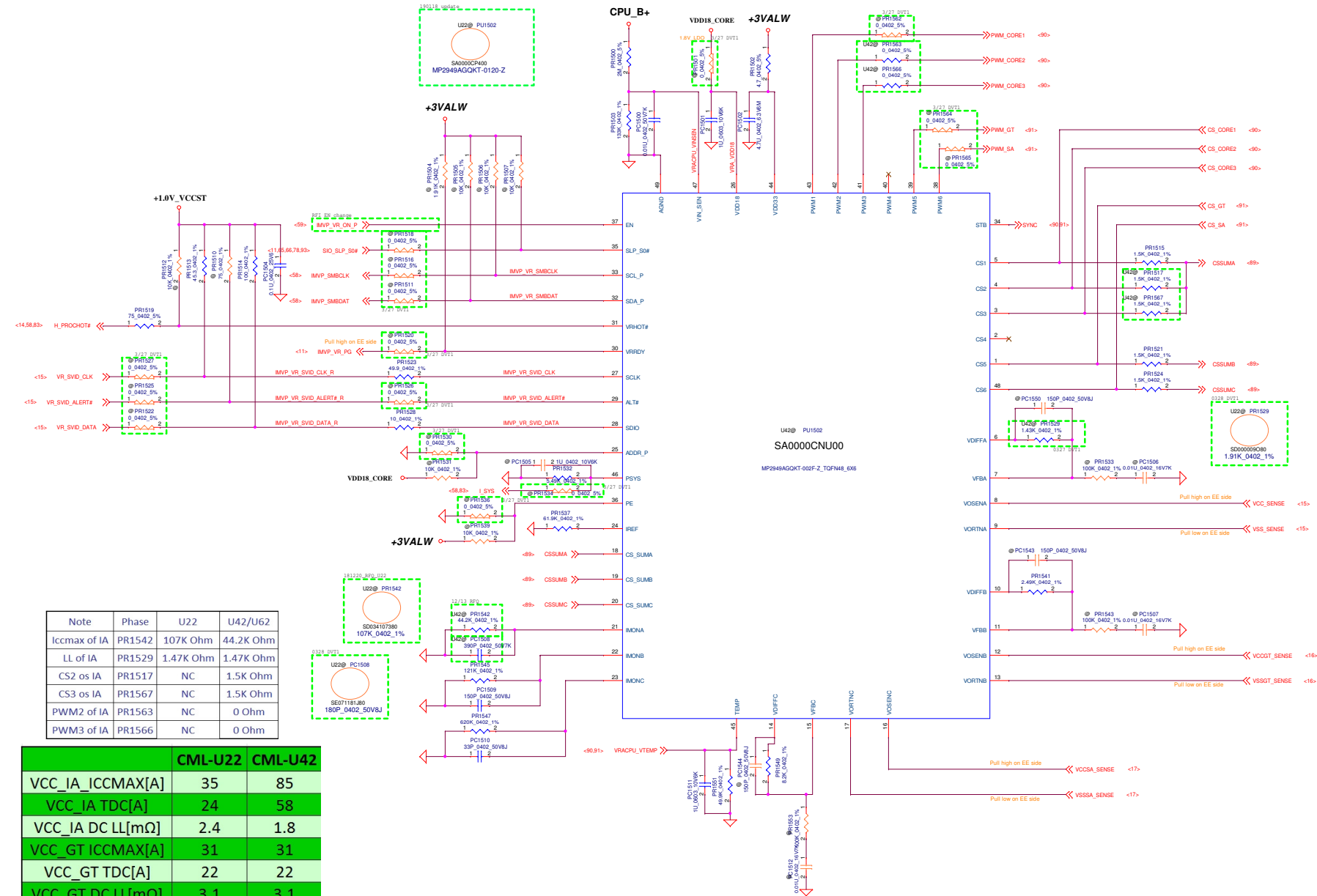
+1.0V\_PRIM\_CORE

+1.0V\_PRIM\_CORE

**PRIM\_CORE**  
TDC 2.98A  
Peak Current 4.26 A  
OCP Current 7.6 A Fix by IC  
MIN:7A  
MAX:8.5A  
Choke DCR 34.0mohm

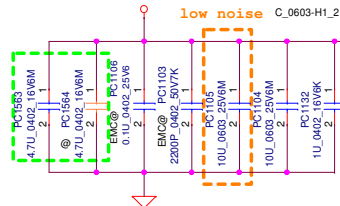
	LPM	VID1	VID0	Vout
	0	X	X	0.75 (LPM)
	1	0	0	0.9
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05

+1.0VS\_VCCIO controller(35.21), Support component(35.22)  
+1.0V\_PRIM\_CORE controller(35.23), Support component(35.24)



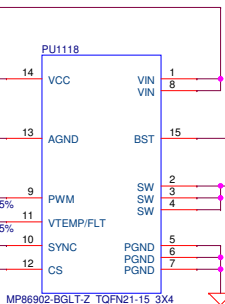
VCC\_CORE Dr. MOS (36.2), Support component(36.3)

CPU\_B+



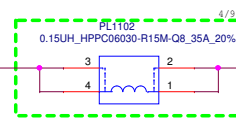
+3VALW

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<89,90,91> VRACPU\_VTEMP  
<89,90,91> SYNC  
<89> CS\_CORE1

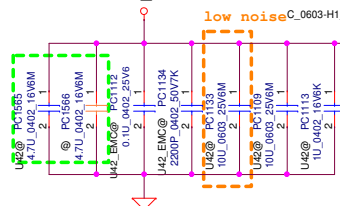


Part No.	Inductance (uH)	Test Freq.	Tolerance (±%)	Irms(A) Max.(Typ)	Isat(A) Max.(Typ)	RDC(mΩ) ±5%
HPCC06030-R15M-Q8	0.15	100kHz,0.5V	20	35(38)	41(45)	0.9

+VCC\_CORE

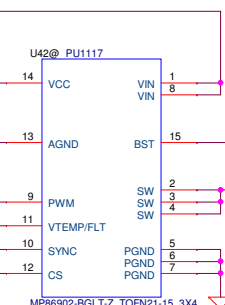


CPU\_B+



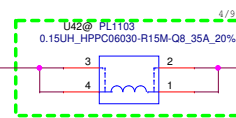
+3VALW

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<89> CS\_CORE2

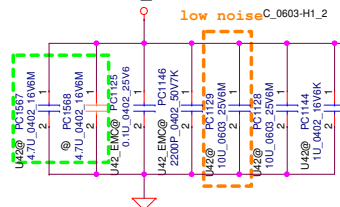


Part No.	Inductance (uH)	Test Freq.	Tolerance (±%)	Irms(A) Max.(Typ)	Isat(A) Max.(Typ)	RDC(mΩ) ±5%
HPCC06030-R15M-Q8	0.15	100kHz,0.5V	20	35(38)	41(45)	0.9

+VCC\_CORE

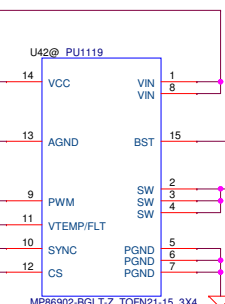


CPU\_B+



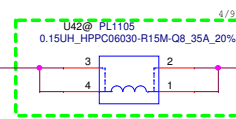
+3VALW

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<89,90,91> SYNC  
<89> CS\_CORE3



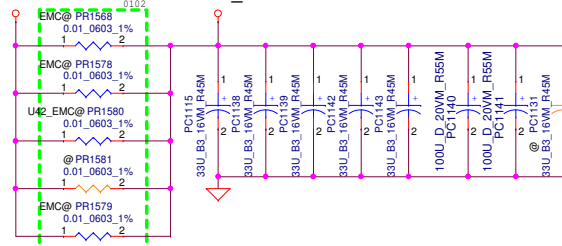
Part No.	Inductance (uH)	Test Freq.	Tolerance (±%)	Irms(A) Max.(Typ)	Isat(A) Max.(Typ)	RDC(mΩ) ±5%
HPCC06030-R15M-Q8	0.15	100kHz,0.5V	20	35(38)	41(45)	0.9

+VCC\_CORE



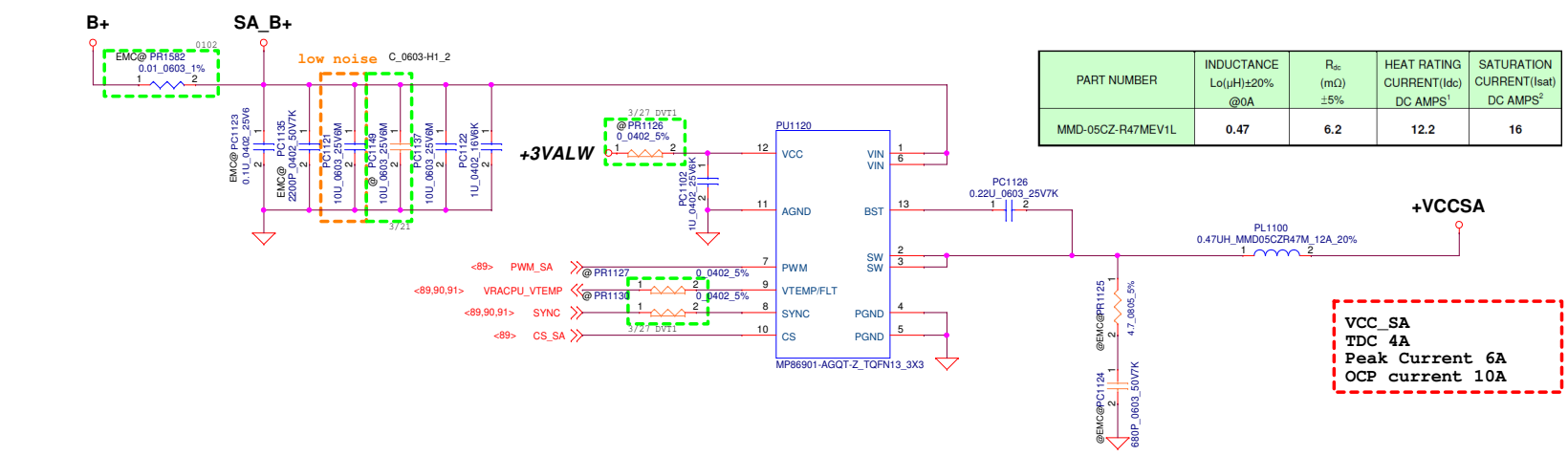
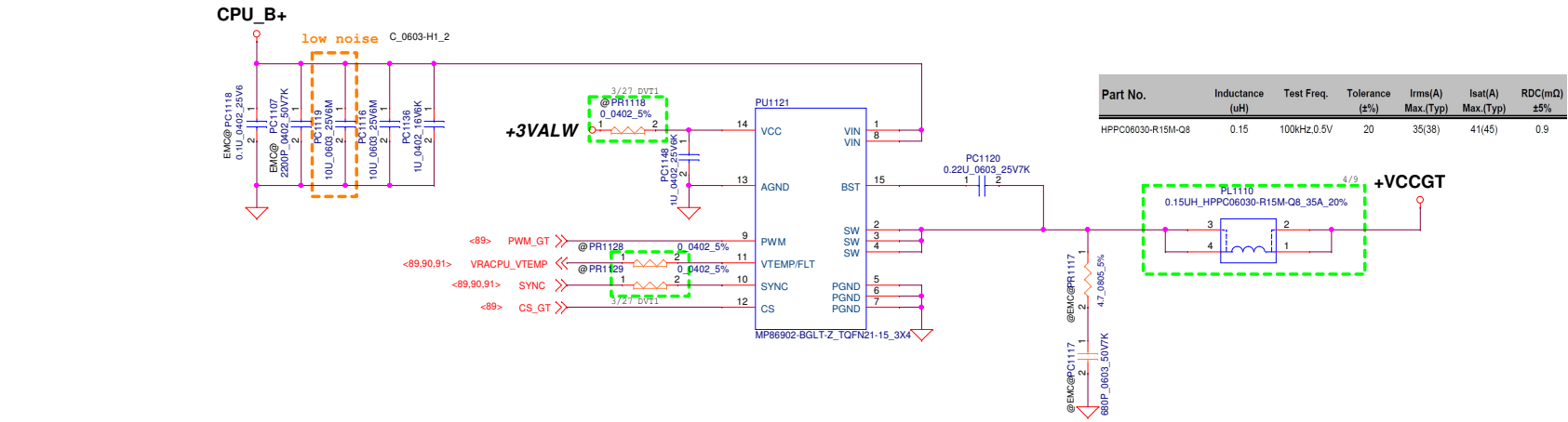
B+

CPU\_B+



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VCC\_GT/SA Dr. MOS (36.2), Support component(36.3)





5					4					3					2					1									
D																													
C																													
B																													
A																													
5					4					3					2					1									
Security Classification					Compal Secret Data										Compal Electronics, Inc.														
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